NCR 53C400
SCSI Host Adapter

General Description

The NCR 53C400 SCSI host adapter chip is a 68-pin CMOS integrated circuit designed to interface the Small Computer Systems Interface (SCSI) bus to an IBM PC, XT, AT or PS/2 model 25, 30 or 30-286 I/O channel bus or compatible. This high performance host adapter circuit retains software compatibility with the NCR 5380/C80 SCSI chip while providing improved asynchronous SCSI bus performance and data buffering to match speeds between the SCSI bus and the host bus. The 53C400 also provides special high-current output drivers capable of sinking 48 mA at 0.5 V, thereby allowing for direct connection to the SCSI bus. This chip can significantly reduce the part count of a SCSI host adapter.

The 53C400 provides an eight-bit interface to the family of IBM PCs and compatibles. It communicates with the host microprocessor as a memory-mapped device. Base memory address is switch selectable between eight choices. The interrupt level of the chip can be programmed for interrupt sharing as required by the PS/2 systems.

Data transfer is accomplished via Programmed Input/ Output (PIO) operation and DMA is thus not required. Speed matching is accomplished by the 53C400 with the use of two 128-byte independent data buffers that can burst data up to the I/O channel's limit. To facilitate the implementation of an external BIOS ROM, a 64-byte scratchpad RAM is included on the chip.

The 53C400 is available in a 68-pin Plastic Leaded Chip Carrier (PLCC) package.

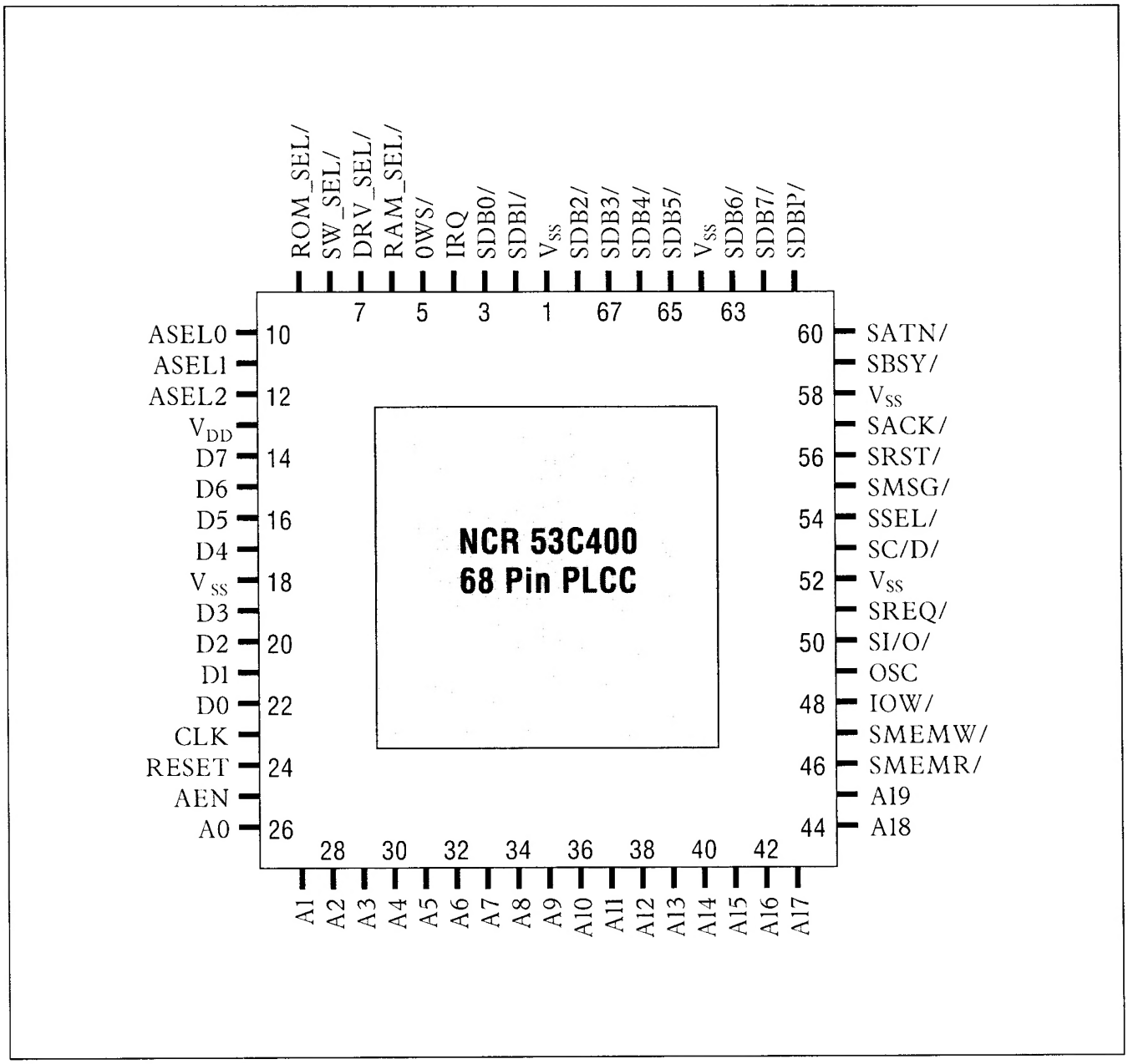
SCSI Interface Features

- ANSI X3.131-1986 compatible
- On-chip 48 mA drivers
- Up to 2.0 MB/S asynchronous SCSI
- Initiator or target roles
- Parity generation, optional checking
- Direct control of SCSI bus signals
- Basic Winchester disk BIOS available

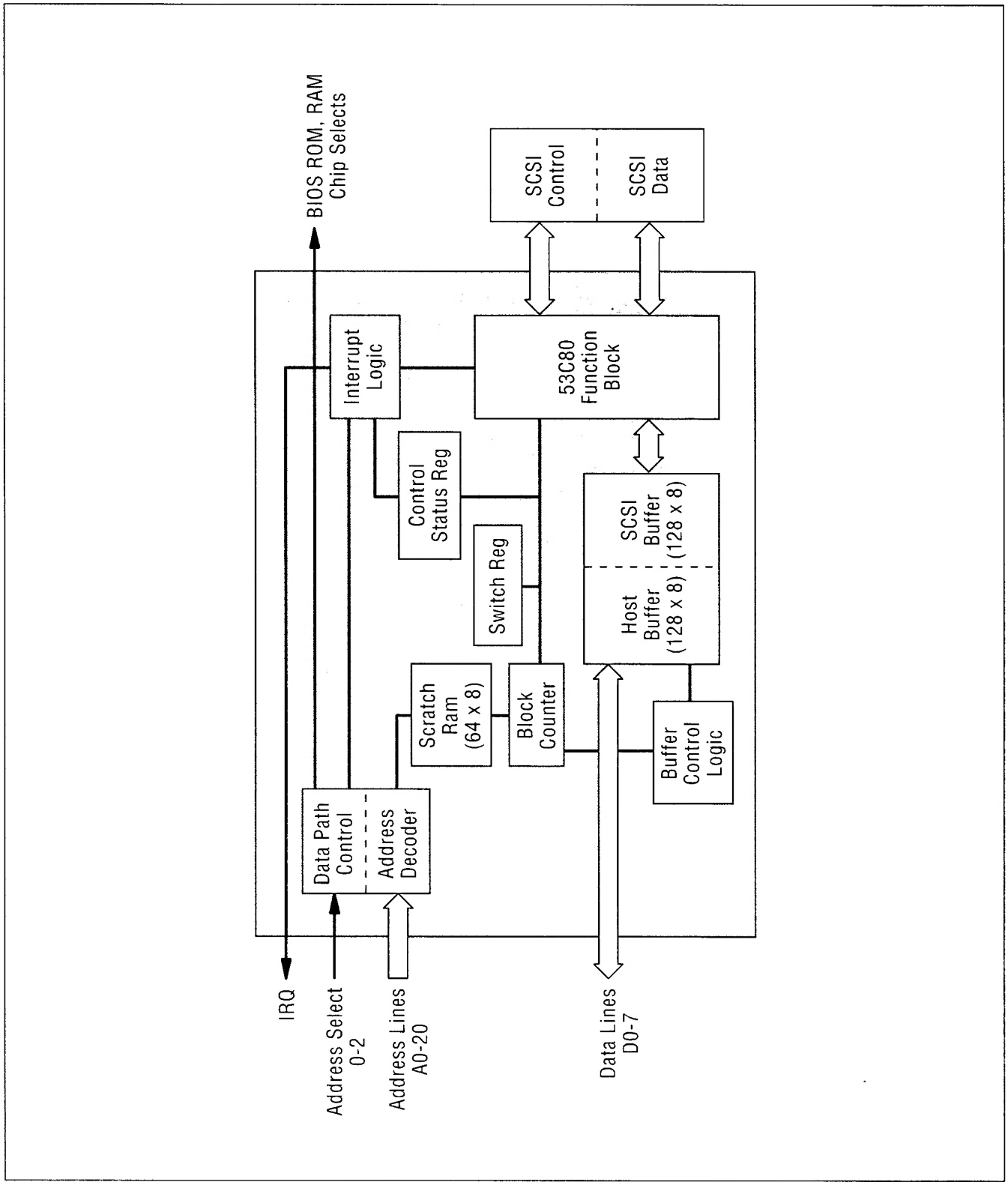
PC (I/O Channel) Interface Features

- Memory-mapped PC interface
- Interrupt/non-interrupt operation
- Switch selectable base memory address
- Programmable interrupt level
- 8-bit data interface
- Two internal 128-byte rotating buffers
- Internal 64-byte scratchpad RAM
- 1.2 MB/S burst transfer rate (6 MHz PC/AT at zero-wait state)

Pin Configuration



Functional Block Diagram



Pin Description

SCSI Interface*

Pin Number	Type	Signal	Description
60	B	SATN/	SCSI attention
59	B	SBSY/	SCSI busy
57	B	SACK/	SCSI acknowledge
56	B	SRST/	SCSI reset
55	B	SMSG/	SCSI message (phase line)
54	B	SSEL/	SCSI select
53	B	SC/D/	SCSI control/data (phase line)
51	B	SREQ/	SCSI request
50	B	SI/O/	SCSI input/output (phase line)
3	B	SDB0/	SCSI data bit 0
2	B	SDB0/	SCSI data bit 1
68	B	SDB0/	SCSI data bit 2
67	B	SDB0/	SCSI data bit 3
66	B	SDB0/	SCSI data bit 4
65	B	SDB0/	SCSI data bit 5
63	B	SDB0/	SCSI data bit 6
62	B	SDB0/	SCSI data bit 7 - has highest priority during arbitration phase
61	B	SDB0/	SCSI data parity - odd parity is used

* *All SCSI bus signals are active-low.*

PC (I/O Channel) Interface

Pin Number	Type	Signal	Description
26-45	I	A0-A19	Active-high address bus which addresses the 53C400's address space. Can be connected directly to the I/O channel.
20-22	B	D2-D0	Active-high data bits 2 through 0 with internal pull-ups.
14-17, 19	B	D7-D3	Active-high data bits 7 through 3.
25	I	AEN	Active-high input signal which de-gates the 53C400 from the I/O channel. When active, the system DMA controller has control of the I/O channel to perform memory refresh.
48	I	IOW/	Active-low write strobe. The only case where the 53C400 decodes this signal is for a rearm of its interrupt (IRQ) in interrupt sharing systems. Refer to *Interrupt Sharing.*
46	I	SMEMR/	Active-low memory read strobe. Address must be valid.
47	I	SMEMW/	Active-low memory write strobe. Address must be valid.
24	I	RESET	Active-high chip reset. This pin has a Schmitt-trigger input. Can be connected directly to the I/O channel.
4	B	IRQ	Active-high interrupt request signal. During normal interrupt mode, this pin has an active pull-up output. In the shared interrupt mode, this pin has an open-drain ouput and a Schmitt-trigger input.
5	O	0WS/	Active-low zero wait-state signal. When active, the micro-processor will not insert extra wait states. Connecting this pin in buses operating above 10 MHz is not recommended.
23	I	CLK	Variable system clock (4.77 MHz to 12 MHz).
49	I	OSC	System oscillator signal of 14.318 MHz.

Miscellaneous

Pin Number	Type	Signal	Description
10-12	I	ASEL0-ASEL2	Active-high base address (segment) select pins. Refer to *Functional Description.*
8	O	SW_SEL/	Active-low external switch register chip select.
9	O	ROM_SEL/	Active-low external ROM chip select.
6	O	RAM_SEL/	Active-low external RAM chip select.
7	O	DRV_SEL/	Active-low external 74LS245 chip select. The 74LS245 transceiver is used to buffer the I/O Channel data bus.
13	-	V_{DD}	+5 V power supply
1, 18, 52, 58, 64	-	V_{SS}	Ground pins. All ground pins except pin 18 are located for connection to the SCSI bus.

Functional Description

The NCR 53C400 is a host adapter chip that along with an external ROM and an optional static RAM can be a complete solution for interfacing the family of IBM PC buses to SCSI.

The main functional blocks of the 53C400 are the 53C80 functional core, host bus decode and interrupt logic, and two 128-byte RAM buffers along with control logic. Also available is a 64-byte scratchpad RAM.

Programming the 53C400 is a two-fold process; (1) the 53C80 core is programmed for all non-data phase SCSI transactions, while (2) the internal control logic for the buffers is programmed for data phase transfers. By allowing the control logic to manage the data phase transfers, a significant gain in throughput can be realized. Refer to the *Programming Flow Chart* for detailed steps.

The 53C400 decodes all 20 memory address-bits from the host system. It provides 8 segment-address selections and each segment occupies a 16 kB of address space. The address segment space of the 53C400 host adapter can be selected by setting switches on the pins A_SEL2, A_SEL1 and A_SEL0.

2	1	0	Segment (hex)
0	0	0	D400
0	0	1	D000
0	1	0	CC00
0	1	1	C800
1	0	0	E400
1	0	1	E000
1	1	0	DC00
1	1	1	D800 (default)

The 53C400 address space (16 kB) is mapped as follows:

Block	Offset
External ROM (14 kB)	0000 - 37FF
Internal SRAM (64-byte)	3800 - 383F
53C80 registers	3880 - 3887
Host buffer (128-byte)	3900 - 397F
Control/status registers	3980 - 3982
External SRAM (1.5 kB)	3A00 - 3FFF

External chip-select signals such as ROM_SEL/ (External Read-Only-Memory Chip Select), RAM_SEL/ (External Static Random-Access-Memory Chip Select), SW_SEL/ (External Switch Register Chip Select) and DRV_SEL/ (External 74LS245 Output Enable) are provided for the convenience of an adapter board implementation. Refer to *Appendix B – Host Adapter Card Layout.*

Data Transfer

Data transfer from the SCSI interface to the host system is accomplished in the following manner. The 53C80 functional core is programmed to facilitate non-block-mode DMA transfer from the SCSI interface to the SCSI buffer, i.e. a 128-byte RAM buffer. The 53C80 core outputs a DMA Request (DRQ) whenever it is ready for a byte transfer. The internal control logic uses this DRQ signal to generate DMA Acknowledge (DACK/) and an IOW/ or IOR/ pulse to the 53C80 core. DRQ will be de-asserted after a required minimum time. This process is repeated for every byte in a transfer from (to) the SCSI buffer. Programmed Input/Output (PIO) is used when the host transfers data from (to) the host buffer, i.e. the second 128-byte RAM buffer.

Simultaneous data transfer i.e. between the SCSI interface and the SCSI buffer and between the host and the host buffer is allowed. For the duration of a transfer, the buffers can be thought of as belonging to their respective interfaces. When both 128-byte buffers complete their data transfer, the control logic switches them to belong to the other interface. A maximum of 256, 128-byte blocks of data, can be transferred during a given transfer period. An 8-bit block counter is to be loaded with the number of blocks initially. This counter decrements by one every time the RAM

buffers switch. When the block counter decrements to zero, an End-Of-Process (EOP/) signal is generated by the control logic to the 53C80 functional core.

The EOP/ signal is not the only way to halt the DMA transfer. A SCSI bus phase mismatch can also terminate a DMA cycle for the current bus phase.

Since the 128-byte buffers do not switch until they are full, non-modulo-128-byte transfers should bypass these buffers and write the data directly to the 53C80 (via PIO).

Zero Wait-State Operation

If the 53C400 is accessed in the offset range of 3800H through 39FFH, the 0WS/ signal is asserted, thereby instructing the microprocessor not to insert any additional wait-states. However, for accesses made to offset space 0000H through 37FFH (external ROM) and to 3A00H through 3FFFH (external RAM), the 0WS/ signal is not asserted and therefore wait-states are added to the read cycle. This feature allows the use of slower external RAMs and ROMs.

For example, a 6 MHz PC/AT uses 3 clock cycles for a memory operation, one of which is a wait-state. Hence, the normal cycle will be 500 nS. By connecting the 0WS/ signal to the I/O channel, the cycle can be reduced to 2 clock cycles or 333 nS. Thus, this feature can significantly improve throughput.

Reset Conditions

Software Chip Reset

When bit 7 of the control status register is set, the 53C400 is reset. All internal logic and control registers are cleared. This is a chip reset only and does not create a SCSI bus reset condition. Also the switch register is not read when this reset occurs.

Hardware Chip Reset

When the signal RESET is active, the 53C400 is reset. The switch register is read following the leading edge of this signal. This is a chip reset only and does not create a SCSI bus reset condition.

SCSI Bus Reset Received

When this signal is received, an interrupt is generated and the 53C80 functional core logic and registers are reset. However, the SCSI SRST/ signal is not latched and therefore may not be present when the current SCSI bus control bits register is read.

SCSI Bus Reset Issued

When bit 7 of the initiator command register is set, the SCSI SRST/ signal (pin 56) goes active and the 53C80 functional core logic and registers are reset. An interrupt is also generated. The SCSI SRST/ will continue to be active until bit 7 of the 53C80 initiator command register is not-set or until a hardware reset occurs.

Interrupt Conditions

The 53C400 can operate in a interrupt/non-interrupt fashion. The interrupts from the 53C80 functional core and the control logic are maskable by setting the appropriate bits in the control status register.

Setting bit 5 of the control status register will enable an interrupt to occur when the SCSI buffer is ready. When writing to the SCSI bus, an interrupt will be generated when the buffer has transferred its contents to the SCSI bus and is ready to switch in the other buffer filled by the host. When reading from the SCSI bus, an interrupt will be generated when the buffer has been filled by data from the SCSI bus and is ready to switch in the other empty buffer. Interrupts generated by this control logic are cleared by reading the control status register.

Asserting bit 4 of the control status register will enable an interrupt to occur when the 53C80 functional core generates an interrupt. Interrupts generated by the 53C80 functional core are maskable to a certain extent based on the event. The following events will cause the 53C80 functional core to generate interrupts: selection/reselection, an occurrence of an EOP/ signal during a DMA transfer (maskable), a SCSI bus reset, a parity error (maskable), an occurrence of a bus phase mismatch, or a SCSI bus disconnection. Interrupts generated by the 53C80 core are cleared by reading register 7 of the 53C80 port or by an external chip RESET (pin 24).

If interrupts are generated by the 53C80 functional core during the data transfer phase, the 53C80 core is automatically unlocked, i.e. bit 7 of the control status register is set. Thus the host can determine the cause of the unexpected interrupt by reading the interrupt status register. If the interrupt is due to a disconnect, a recovery scheme is implemented as explained in *Disconnect Operation.*

When the control logic issues an EOP/ pulse to the 53C80, i.e. when the block counter decrements to zero, reading bit 7 of the interrupt status register will confirm that the DMA transfer is complete.

Interrupt Sharing

In systems utilizing shared interrupts (as in the PS/2 model 30), interrupts are cleared by writing to the I/O address 02Fx, where x is the interrupt level set in bits 2-0 of the switch register. (Refer to *Switch Register* for setting descriptions.) This is the only instance where the IOW/ input is used by the 53C400.

Initialization

Initialization of the 53C400 involves setting the pins ASEL2 - 0 to the correct segment address. Upon resetting the 53C400, the 53C400 will strobe in the contents of an optional switch register, thereby determining which interrupt level is to be used.

Initialization of the 53C80 functional core is determined by the firmware and is up to user discretion. Bits in the control status register will have to be set as desired.

As part of the system initialization, the 53C400 BIOS should query the number and types of SCSI IDs and LUNs connected to the host adapter. A device table is usually established that the operating system can recognize. Allowances for device spin-up and unit ready status must be made.

SCSI Disconnect Operation

The 53C400 allows the disconnection and reconnection by SCSI devices transferring data to or from it. A target will disconnect by issuing an optional save data pointers message and a mandatory disconnect message to the 53C400. The target will then de-assert BSY/, thereby placing the SCSI bus in a bus free state. To allow reselection by the target, the 53C400 should be set up to enable selection by writing its SCSI ID to the select enable register. Also parity checking is recommended to eliminate false selections.

If it is necessary to transfer control back to the operating system during the time lapse between disconnect and reconnect, the hardware interrupt should be enabled via the control status register. Thus, the 53C400 will generate an interrupt during the selection and an interrupt service routine can reestablish the logical thread.

In the event of a disconnect by the target during the data transfer phase, if the same logical unit reconnects to the 53C400, then data transfer can be resumed from the point of disconnect. This is done by performing a dummy write to the switch register after the correct SCSI data phase has been reestablished.

Register Set

53C80 Registers

The NCR 53C80 core appears as a set of eight registers to the controlling microprocessor. By reading and writing the appropriate registers, the microprocessor may initiate SCSI protocol activity or may sample and assert any signal on the SCSI bus. These registers must be read/written only when the 53C80 register access bit (bit 7) of the control status register is true.

Bits in registers which correspond to active-low SCSI signals appear as set (logic 1) when the SCSI signal is asserted (logic 0).

Refer to *Appendix B – Register Summary.*

Current SCSI Data Register Read Address 3880H

The current SCSI data register is a read-only register which allows the microprocessor to monitor the active SCSI data bus. If parity checking is enabled, the SCSI bus parity is checked at the beginning of the read cycle. This register is used during arbitration to check for higher priority arbitrating devices. Parity is not guaranteed valid during arbitration.

Output Data Register Write Address 3880H

The output data register is a write-only register that sends data to the SCSI bus. This register is also used to assert the proper ID bits to drive the SCSI bus during the arbitration and selection phases.

Initiator Command Register Read/Write Address 3881H

The initiator command register is a read/write register which asserts certain SCSI bus signals, monitors those signals, and monitors the progress of SCSI bus arbitration.

Bit 7 (Assert RST/ - read/write)
When set, the SRST/ signal is asserted on the SCSI bus. The SRST/ signal will remain asserted until this bit is reset or until RESET/ (pin 24) is asserted. After this bit is set, IRQ goes active and all SCSI signals are removed except for SRST/. Registers 3880H - 3887H are reset. This bit must be reset by the host to de-assert the SRST/ signal.

Bit 6 (Arbitration in progress - read only)
This bit is used to determine if arbitration is in progress. For this bit to be active, the arbitrate bit (register 3882H, bit 0) must have previously been set. The arbitration in progress bit indicates that a bus-free condition has been detected and that the chip has asserted SBSY/ and the contents of the output data register onto the SCSI bus. Arbitration in progress will remain set until the abritrate bit is reset.

Bit 6 (Test mode - write only)
This bit may be set in a test environment to disable all output drivers of the 53C400.

Bit 5 (Lost arbitration - read only)
When set, this bit indicates that the chip has detected a bus-free condition, arbitrated for use of the bus by asserting SBSY/ and its ID on the SCSI bus and lost arbitration due to SSEL/ being asserted by another bus device. For this bit to be set, the arbitrate bit (register 3882H, bit 0) must be set.

Bit 4 (Assert ACK/ - read/write)
This bit is used by the initiator to assert SACK/ onto the SCSI bus. In order to assert SACK/, the target mode bit (register 3882H, bit 6) must not be set. Writing a zero to this bit de-asserts SACK/ on the SCSI bus. Reading this register simply reflects the status of this bit.

Bit 3 (Assert BSY/ - read/write)
When set, this bit asserts SBSY/ onto the SCSI bus. When reset, this bit de-asserts the SBSY/ signal. Asserting SBSY/ indicates a successful selection or reselection and resetting this bit creates a bus-disconnect condition. Reading this register simply reflects the status of this bit.

Bit 2 (Assert SEL/ - read/write)
When set, this bit asserts SSEL/ onto the SCSI bus. SSEL/ is normally asserted after arbitration has been successfully completed. When reset, this bit de-asserts the SSEL/ signal. Reading this register simply reflects the status of this bit.

Bit 1 (Assert ATN/ - read/write)
When set, this bit asserts SATN/ onto the SCSI bus if the target mode bit (register 3882H, bit 6) is not set. SATN/ is normally asserted by the initiator to request a message out phase. When reset, this bit de-asserts the SATN/ signal. Reading this register simply reflects the status of this bit.

Bit 0 (Assert data bus - read/write)
When set, this bit allows the contents of the output data register to be enabled as chip outputs on SCSI signals SDB0/ to SDB7/. Parity is also generated and asserted on SDBP/. When connected as an initiator, the outputs are only enabled if the target mode bit (register 2, bit 6) is not set, and the phase signals SC/D/, SI/O/, and SMSG/ match the contents of the assert C/D/, assert I/O/, and assert MSG/ in the target command register. The assert data bus bit should also be set during DMA operations.

Mode Register Read/Write Address 3882H

The mode register is used to control the operation of the 53C80 block of the chip. This register determines whether the chip operates as an initiator or target, whether parity is checked, and whether interrupts are generated on various external conditions.

Bit 7 (Block mode DMA)
Block mode DMA is not allowed in the 53C400 and hence this bit must never be asserted. If this bit is mistakenly set, the internal DMA logic between the 53C80 and the SCSI buffer will not operate correctly.

Bit 6 (Target mode - read/write)
Asserting this bit places the 53C400 in a target mode.

Bit 5 (Enable parity checking - read/write)
This bit determines whether parity errors will be ignored or saved in the parity error latch. When set, parity errors are saved. When reset, parity errors are ignored.

Bit 4 (Enable parity interrupt - read/write)
When set, this bit causes the 53C80 IRQ signal to be asserted if a parity error is detected. A parity interrupt will only be generated if the enable parity checking bit (bit 5) is also set. This 53C80 IRQ signal is passed on to the IRQ pin (pin 4) only if bit 4 of the 53C400 control status register is set.

Bit 3 (Enable EOP interrupt - read/write)
When set, this bit causes the 53C80 IRQ signal to be asserted when an End-Of-Process (EOP/) signal is received from the internal DMA logic.

Bit 2 (Monitor busy - read/write)
When set, this bit causes the 53C80 IRQ signal to be asserted when BSY/ unexpectedly changes from active to inactive. When the interrupt is generated, the lower six bits of the initiator command register are reset and all signals are de-asserted on the SCSI bus. The busy error bit (register 3885H, bit 2) will also be set when this condition occurs.

Bit 1 (DMA mode - read/write)
The DMA mode bit allows a DMA transfer to occur and must be set prior to writing registers 3885H to 3887H. These registers are used to start DMA transfers. The target mode bit (register 3882H, bit 6) must be set for a write to register 3886H and reset for a write to register 3887H. The assert data bus bit (register 3881H, bit 0) must be set for all DMA send operations. In the DMA mode, SREQ/ and SACK/ are automatically controlled.

Bit 0 (Arbitrate - read/write)
When set, this bit starts the arbitration process when a bus-free condition has been detected. Prior to setting this bit the output data register should contain the proper SCSI device ID value. One SCSI ID bit should be active for SCSI bus arbitration. The chip will wait for a bus-free condition before entering the arbitration phase. The status of the arbitration phase may be determined by reading the lost arbitration and arbitration in progress bits (register 3881H, bits 5 and 6 respectively).

Target Command Register Read/Write Address 3883H

The target command register, when connected as a target device, allows the microprocessor to control the SCSI bus information transfer phase.

Bit 7 (Last byte sent - read only)
This bit indicates that the last byte of the DMA operation has been sent on the SCSI bus. This flag is necessary since the end of DMA transfer bit (register 3885H, bit 7) only reflects when the last byte was received from the DMA controller. This bit is cleared if the DMA mode bit (register 3882H, bit 1) is reset.

Bit 6 (Reserved; must be written to zero.)

Bit 5 (Reserved; must be written to zero.)

Bit 4 (Reserved; must be written to zero.)

Bit 3 (Assert REQ/ - read/write)
When this bit is set and the 53C80 is configured as a target, the SCSI REQ/ will be active.

Bit 2 (Assert MSG/ - read/write)
When this bit is set, the SCSI MSG/ will be active. This bit must be set to match the expected SCSI phase (determined by the target) if a phase mismatch interrupt is required.

Bit 1 (Assert C/D/ - read/write)
When this bit is set, the SCSI C/D/ will be active. This bit must be set to match the expected SCSI phase (determined by the target) if a phase mismatch interrupt is required.

Bit 0 (Assert I/O/ - read/write)
When this bit is set, the SCSI I/O/ will be active. This bit must be set to match the expected SCSI phase (determined by the target) if a phase mismatch interrupt is required.

Current SCSI Control Bits Register Read Address 3884H

The current SCSI control bits register is a read-only register which monitors seven SCSI bus control signals plus the SCSI data bus parity bit. These bits are not latched.

When a bit is set, it represents an asserted signal on the SCSI bus.

Bit 7 (SRST/)

Bit 6 (SBSY/)

Bit 5 (SREQ/)

Bit 4 (SMSG/)

Bit 3 (SC/D/)

Bit 2 (SI/O/)

Bit 1 (SSEL/)

Bit 0 (SDBP/)

Select Enable Register Write Address 3884H

The select enable register is a write-only register which masks all but a single ID bit during a selection attempt. The SCSI ID to be monitored is written as a one (1) in the register. For example, if SCSI ID 7 is to be selected, then bit 7 must be set for the 53C80 interrupt to be generated after a successful selection. The simultaneous occurrence of the correct SCSI ID, SBSY/ inactive, and SSEL/ active will cause an interrupt. This interrupt can be disabled by resetting all bits in this register. If the enable parity checking bit (register 2, bit 5) is active, parity will be checked during selection.

Interrupt Status Register Read Address 3885H

The interrupt status register is a read-only register which monitors six (6) status bits and the two SCSI control signals (SATN/ and SACK/ which are not found in the current SCSI control bits register (register 3884H).

Bit 7 (End of DMA transfer)
This bit is set if the 53C80 EOP/, DACK/, and IOR/ or IOW/ are simultaneously active for at least 100 nS. The EOP/ signal is generated by the logic external to the 53C80 core at the end of the complete transfer. The last byte sent bit (register 3883H, bit 7) must be monitored to ensure that the last byte sent to the output data register (register 3880H) has been transferred to the SCSI bus. This bit is reset when the DMA mode bit (register 3882H, bit 1) is reset.

Bit 6 (DMA request)
This bit allows the microprocessor to sample the 53C80 DRQ signal. DRQ can be cleared by asserting the DACK/ signal or by resetting the DMA mode bit (register 3882H, bit 1). The DRQ signal does not reset when a 53C80 phase mismatch interrupt occurs. DRQ is cleared by control logic external to the 53C80 core, during block transfers.

Bit 5 (Parity error)
This bit is set if a parity error occurs when receiving data or during a device selection. It can only be set if the enable parity checking bit (register 3882H, bit 5) is set. This bit may be cleared by reading the reset parity/interrupt register (register 3887H).

Bit 4 (Interrupt request active)
This bit is set by the 53C80 when an interrupt condition has been detected. It reflects the current state of the 53C80 IRQ signal and can be cleared by reading the reset parity/interrupt register (register 3887H). Refer to *Interrupt Conditions.*

Bit 3 (Phase match)
The SCSI SMSG/, SC/D/, and SI/O/ signals represent the current information transfer phase. The phase match bit indicates whether the current SCSI bus phase matches the lower three (3) bits of the target command register (register 3883H). The phase match bit is continuously latched and updated and is only significant when operating as a bus initiator. A phase match is required for data transfer to occur on the SCSI bus.

Bit 2 (Busy error)
This bit is active if an unexpected change of the SBSY/ signal has occurred. This level-sensitive latch is set whenever the monitor busy bit (register 3882H, bit 2) is set and SBSY/ is detected inactive. The busy error bit will disable any SCSI outputs and will reset the DMA mode bit (register 3882H, bit 1).

Bit 1 (ATN/)
This bit reflects the condition of the SCSI SATN/ signal. When this bit is set, SATN/ is active. This signal is normally monitored by the target device.

Bit 0 (ACK/)
This bit reflects the condition of the SCSI bus control signal SACK/. When this bit is set, SACK/ is active. This signal is normally monitored by the target device.

Start DMA Send Register Write Address 3885H

The Start DMA send register is a write-only register that produces a strobe which starts a DMA send from the chip to the SCSI bus. To initiate a DMA send operation, the DMA mode bit (register 3882H, bit 1) must be set. Any value written to this register will start the DMA send operation. The DMA send operation can be initiated in either the initiator or the target mode.

Input Data Register Read Address 3886H

The input data register is a read-only register that is used to receive data from the SCSI bus during DMA transfers. In the initiator mode, data is latched in on the falling edge of SREQ/, whereas in the target mode, data is latched in on the falling edge of SACK/. The contents of this register represent the complement of the active low SCSI data bus.

Start DMA Target Receive Register Write Address 3886H

The start DMA target receive register is written to initiate a DMA receive from the SCSI bus to the chip for target operation only. The DMA mode bit and the target mode bit (register 3882H, bits 1 and 6) must be set prior to writing this register. Any value written to this register will start the DMA send operation.

Reset Interrupt Register Read Address 3887H

The reset parity/interrupt register is a read-only register which, when read, resets the parity error bit, the interrupt request bit, and the busy error bit in the interrupt status register (register 3885H). Reading this register will de-assert the 53C80 IRQ signal.

Start DMA Initiator Receive Register Write Address 3887H

The start DMA initiator receive register is a write-only register which, when written to, initiates a DMA receive from the SCSI bus to the chip for initiator operation only. To initiate a DMA initiator receive operation, the DMA mode bit (register 3882H, bit 1) must be set and the target mode bit (register 3882H, bit 6) must not be set. Any value written to this register will start the DMA initiator receive operation.

Control Status Register Read/Write Address 3980H

Bit 7 (Reset - write only)
Asserting this bit will reset the 53C400.

Bit 7 (53C80 Register access - read only)
When this bit is set by the 53C400 logic, the 53C80 registers can be accessed. This bit will be set to zero when data is being transferred between the 53C80 and the SCSI buffer by the 53C400 logic. Following a data transfer, this bit should be polled before trying to access a 53C80 register.

Bit 6 (Data transfer direction)
0 = write data, 1 = read data. Setting this bit will initiate data transfer from the SCSI port to the host, while not-setting this bit will initiate data transfer from the host to the SCSI port.

Bit 5 (Enable SCSI buffer interrupt)
Asserting this bit will enable an interrupt (IRQ) to occur when the SCSI buffer is ready to transfer, i.e. bit 1 of this register is asserted.

Bit 4 (Enable 53C80 interrupt)
Asserting this bit will enable an interrupt (IRQ) to occur when the 53C80 function block asserts its IRQ signal, i.e. bit 0 of this register is asserted.

Bit 3 (Shared interrupt)
Asserting this bit allows multiple adapters to share an interrupt level as implemented in the IBM PS/2 model 30.

Bit 2 (Host buffer not ready - read only)
When set, this bit indicates that the host buffer is either not ready to accept data when writing from the host to the SCSI bus, or not ready to supply data when being read by the host.

Bit 1 (SCSI buffer ready - read only)
When set, this bit indicates that the current SCSI buffer is empty and ready to switch in the next full buffer when writing from the host to the SCSI bus; or the current SCSI buffer is full and ready to switch in an empty buffer when being read by the host. This bit is latched and cleared when this register is read.

Bit 0 (Gated 53C80 IRQ - read only)
This bit reflects the state of the 53C80 core IRQ signal. When in an initiator read mode, this signal is delayed until the last block has been transferred to the host memory.

Block Counter Register Read/Write Address 3981H

This 8-bit read/write register should be loaded with the number of 128-byte blocks of data to be transferred. An hexadecimal value of 00 indicates 256 blocks to be transferred. Loading this register will also initiate data transfer from (to) the SCSI bus to (from) the SCSI buffer in the 53C400.

Switch Register Read Address 3982H

This 8-bit read/write register is used for two purposes. At initialization the 53C400 can be configured through optional external hardware switches for bits 7 through 0. The values of the switches are strobed in following a reset.

Bits 7 through 3 are user-defined by setting the appropriate hardware switches. For example, the chip's SCSI ID can be set with these switches. Bits 2 through 0 are reserved in the interrupt-sharing systems to indicate the interrupt level of the host adapter as follows:

2	1	0	Interrupt level
0	0	0	N/A
0	0	1	N/A
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7 (default)

Resume Transfer Register Write Address 3982H

The purpose for this register is to resume data transfer in the case of an occurrence of a SCSI disconnect/reconnect during the data transfer phase. A dummy write to this register restarts the data transfer from the point of disconnect.

External BIOS ROM Read Address 0000H - 37FFH

A 14 kB external basic I/O System (BIOS) ROM module can be implemented by the designer to contain routines needed to perform SCSI operations such as arbitration and selection, commands, data transfer, message and status. The 53C400 provides a chip-select signal, ROM_SEL/, to enable this ROM.

The host system will recognize this module and establish its interrupt vectors once Power On Self Test (POST) has begun. To be valid, the ROM will have to be defined as follows:

Byte 0
55 hex

Byte 1
AA hex

Byte 2
A length indicator representing the number of 512-byte blocks in the ROM

Byte 3
Executable code

When POST identifies a valid ROM, it does a far call to byte 3 of the ROM and the executable code at this address should perform its power-on initialization tasks. Refer to *Initialization.* The ROM should then return control to the system BIOS routines by executing a far return. Please refer to the *IBM Technical Reference Manuals* for further information.

Host Buffer Port R/W Address 3900H - 397FH

This internal 128-byte buffer contains data received from the SCSI bus during a read by the host and this buffer should be written by the host during a write to the SCSI bus. Although the host buffer is mapped into memory from offset address 3900H to 397FH (128-byte), this buffer in actuality emulates a stack. If desired the host can transfer the entire 128 bytes to a single address within this address mapping. The primary reason for mapping this buffer to 128 bytes is to accommodate the memory move block instructions.

An internal up-down counter will keep count of how many bytes have been transferred. When it reaches 128, it will rotate this buffer with the SCSI buffer.

Because of the stack nature of this buffer and rotation with the SCSI buffer when full, data written to the buffer cannot be read back.

Internal Scratchpad RAM R/W Address 3800H - 383FH

This 64-byte memory space may be used by the ROM routines as scratchpad space for any calculations or temporary storage. This SRAM is not a FIFO and individual addresses need to be generated for each byte to be stored or read.

External Static Ram R/W Address 3A00H - 3FFFH

This optional 1.5 kB external static RAM may be used by the ROM routines as scratchpad space for any calculations if the internal RAM space is insufficient. The 53C400 provides a chip-select signal RAM_SEL/, to enable this RAM.

DC Characteristics

Absolute Maximum Stress Ratings

Parameter	Symbol	Minimum	Maximum	Unit
Storage temperature	T_{STG}	-55	150	°C
Supply voltage	V_{DD}	-0.5	7.0	V
Input voltage	V_{IN}	V_{SS}-0.5	V_{DD}+0.5	V
Electrostatic discharge sensitivity	ESD*	-	4000	V
Latch-up sensitivity	LUS**	-	100	mA

** Test using the human body model (100 pF at 1.5K ohms).*

*** Test using current-limited power supply, voltage ramp from V_{DD} to V_{DD}+ 0.5 and vlotage ramp from V_{SS} to V_{SS}- 0.5.*

Operating Conditions

Parameter	Symbol	Minimum	Maximum	Unit
Supply voltage	V_{DD}	4.75	5.25	V
Supply current	I_{DD}	-	50	mA
Operating free-air temperature	T_A	0	70	°C

SCSI Bidirectional Lines (pins 2, 3, 50, 51, 53-55, 57, 59-63, 65-68)

Parameter	Symbol	Conditions	Min	Max	Unit
Input high voltage	V_{IH}	-	2.0	V_{DD} + 0..5	V
Input low voltage	V_{IL}	-	V_{SS} - 0.5	0.8	V
Output low voltage	V_{OL}	I_{OL} = 48 mA	V_{SS}	0.5	V
Input high leakage	I_{IH}	$V_{IH} = V_{DD}$	-	10	µA
Input low leakage	I_{IL}	$V_{IL} = V_{SS}$	-	-50	µA

IRQ (pin 4)

Parameter	Symbol	Conditions	Min	Max	Unit
Output low voltage	V_{OL}	I_{OL} = 16 mA	V_{SS}	0.4	V
Output high voltage	V_{OH}	I_{OH} = - 16 mA	2.4	V_{DD}	V
Input high leakage	I_{IH}	$V_{IH} = V_{DD}$	-	10	µA
Input low leakage	I_{IL}	V_{IL} = 0 V	-	-10	µA

SRST/ (pin 56)

Parameter	Symbol	Conditions	Min	Max	Unit
Input high voltage	V_{IH}	-	2.2	V_{DD}+0.5	V
Input low voltage	V_{IL}	-	V_{SS}-0.5	0.8	V
Output low voltage	V_{OL}	I_{OL} = 48 mA	V_{SS}	0.5	V
Input high leakage	I_{IH}	$V_{IH} = V_{DD}$	-	10	µA
Input low leakage	I_{IL}	$V_{IL} = V_{SS}$	-	-750	µA

OWS (pin 5)

Parameter	Symbol	Conditions	Min	Max	Unit
Output low voltage	V_{OL}	I_{OL} = 16 mA	V_{SS}	0.4	V

RAM_SEL/, DRV_SEL/, SW_SEL/, ROM_SEL/ (pins 6-9)

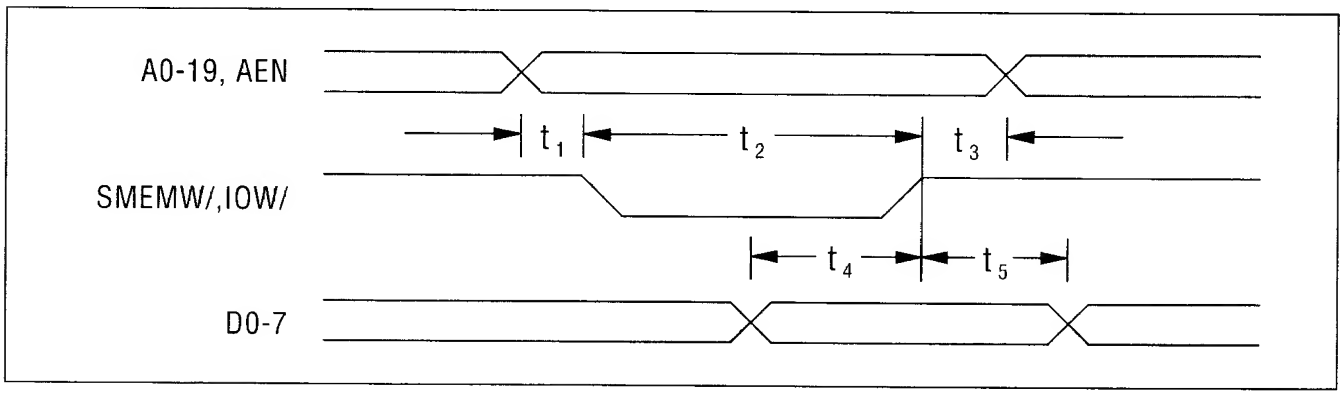
Parameter	Symbol	Conditions	Min	Max	Unit
Output low voltage	V_{OL}	I_{OL} = 2 mA	V_{SS}	0.4	V
Output high voltage	V_{OH}	I_{OH} = - 2 mA	2.4	V_{DD}	V

All Other Pins

Parameter	Symbol	Conditions	Min	Max	Unit
Input high voltage	V_{IH}	-	2.0	V_{DD} + 0.5	V
Input low voltage	V_{IL}	-	V_{SS} - 0.5	0.8	V
Output high voltage	V_{OH}	I_{OH} = - 4 mA	2.4	V_{DD}	V
Output low voltage	V_{OL}	I_{OL} = 4 mA	V_{SS}	0.4	V
Input high leakage	I_{IH}	$V_{IH} = V_{DD}$	-	10	µA
Input low leakage	I_{IL}	V_{IL} = 0 V	-	-10	µA
For A_SEL 2:0	-	-	-	-2.5	mA
For D2 - D0	-	-	-	-1.2	mA

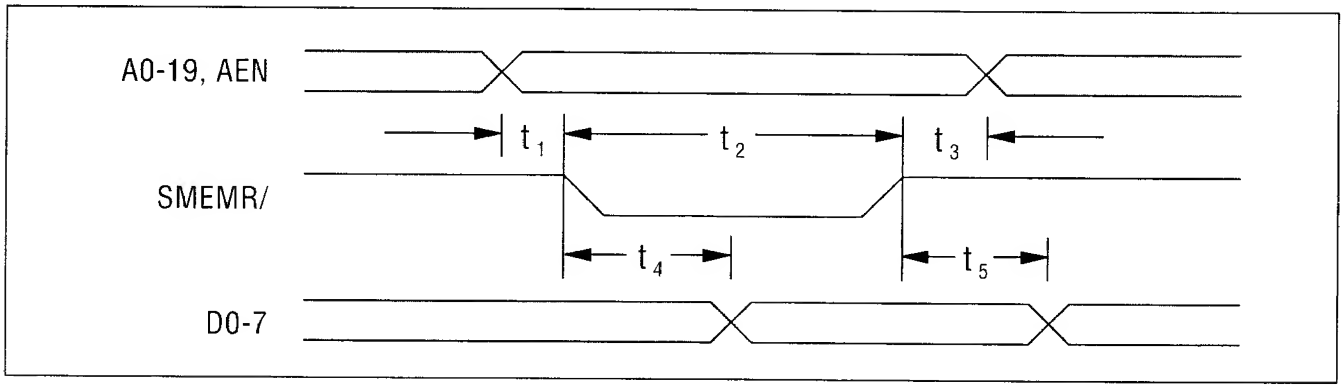
AC Characteristics

CPU Write



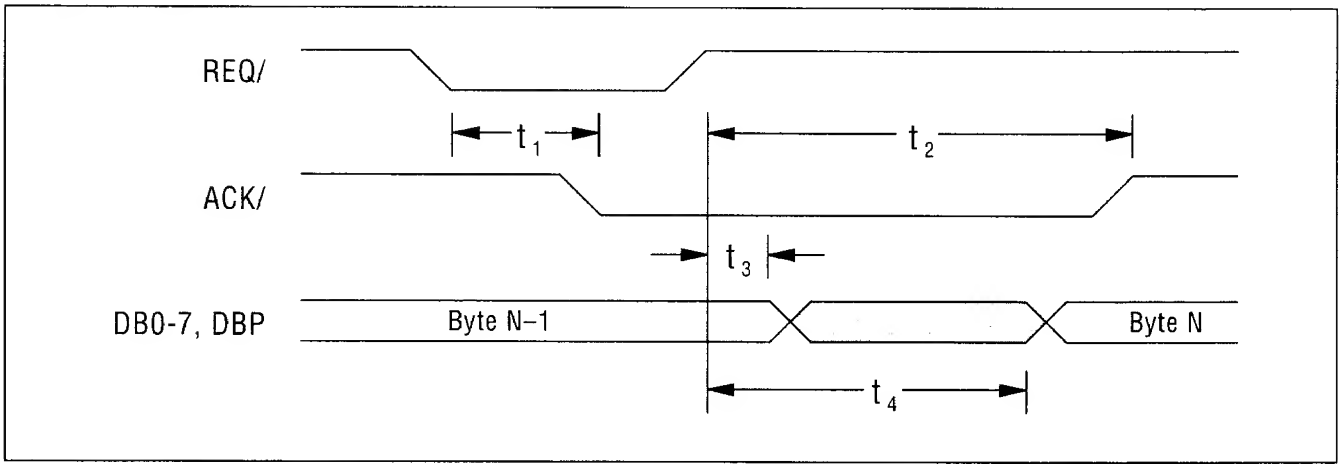
Parameter	Symbol	Minimum	Maximum	Unit
Address setup to write enable	t_1	35	-	nS
Write enable width	t_2	80	-	nS
Address hold from end of write enable	t_3	25	-	nS
Data setup to end of write enable	t_4	25	-	nS
Data hold from end of write enable	t_5	30	-	nS

CPU Read



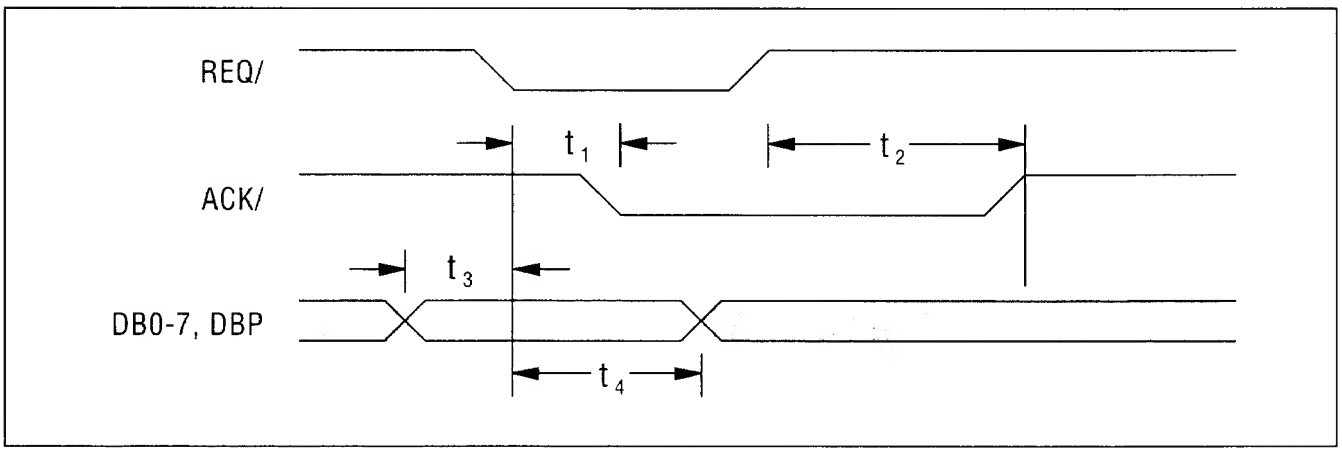
Parameter	Symbol	Minimum	Maximum	Unit
Address setup to read enable	t_1	35	-	nS
Read enable width	t_2	125	-	nS
Address hold from end of read enable	t_3	25	-	nS
Data access time from read enable	t_4	-	120	nS
Data disable from end of read enable	t_5	5	-	nS

SCSI Write (Non-block mode) – Initiator Send



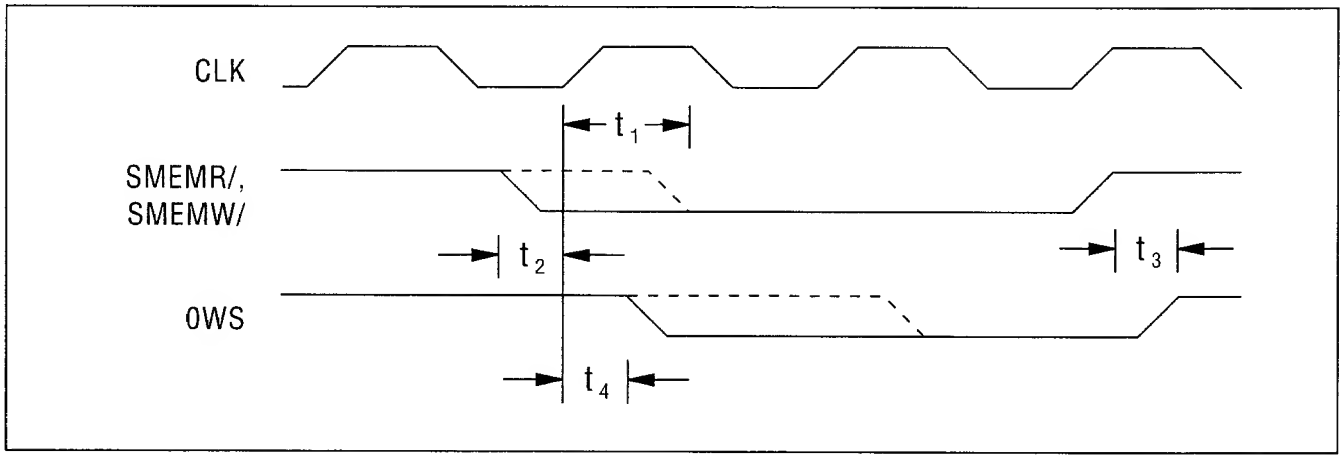
Parameter	Symbol	Minimum	Maximum	Unit
REQ/ true to ACK/ true	t_1	-	55	nS
REQ/ false to ACK/ false	t_2	-	380	nS
Previous data disable from REQ/ false	t_3	60	225	nS
REQ/ false to valid SCSI data	t_4	70	260	nS

SCSI Read (Non-block mode) – Initiator Receive



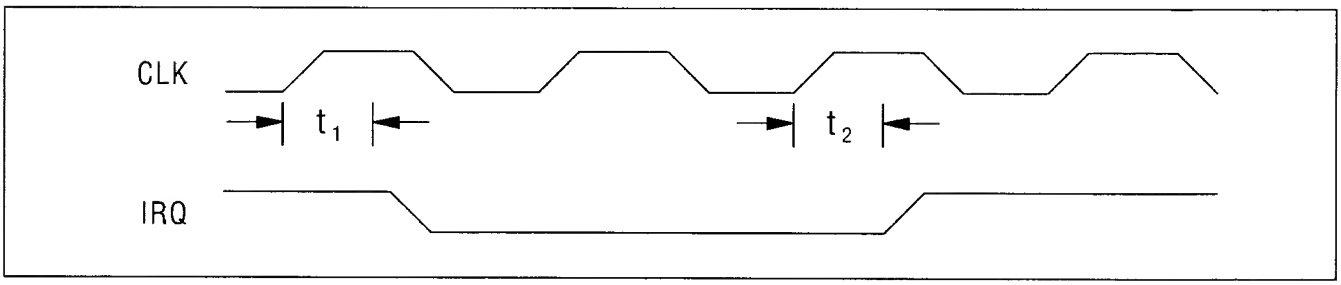
Parameter	Symbol	Minimum	Maximum	Unit
REQ/ true to ACK/ true	t_1	-	50	nS
REQ/ false to ACK/ false	t_2	-	100	nS
SCSI data setup to REQ/ true	t_3	20	-	nS
SCSI data disable from REQ/ true	t_4	50	-	nS

0WS Timing



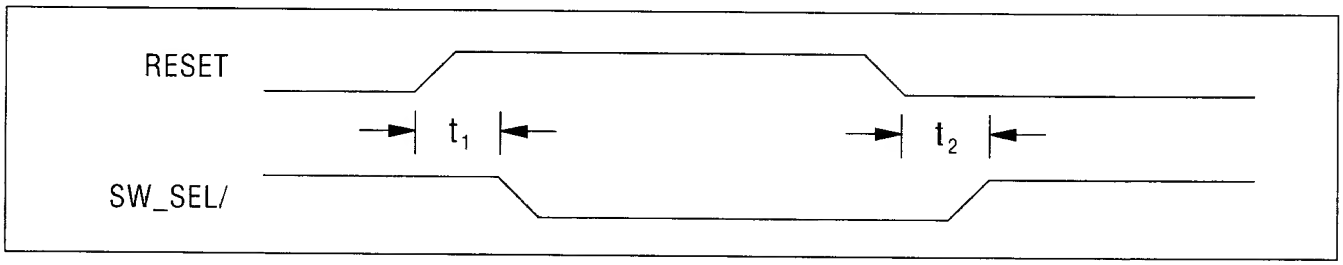
Parameter	Symbol	Minimum	Maximum	Unit
Read or write enable hold time from rising CLK	t_1	2	-	nS
Read or write enable setup time to rising CLK	t_2	14	-	nS
0WS trailing edge delay from read/write false	t_3	-	35	nS
0WS leading edge delay from rising CLK	t_4	-	30	nS

Shared IRQ Timing



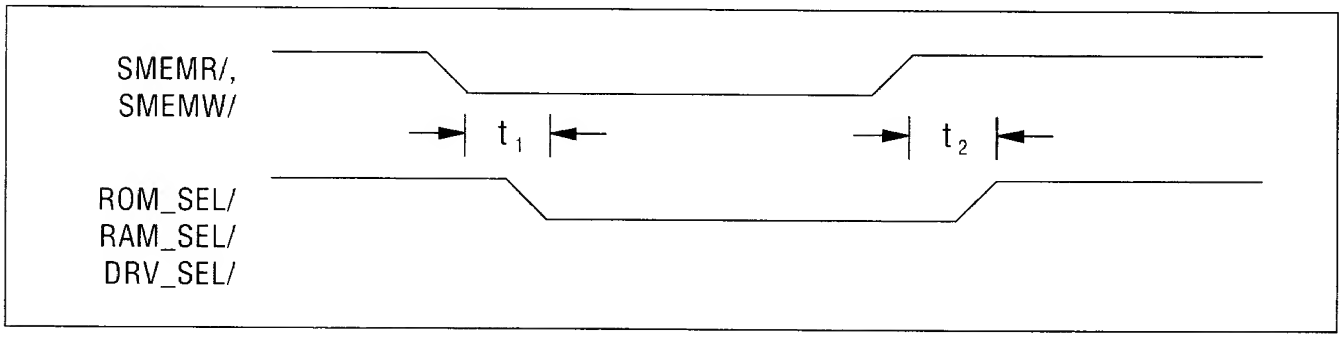
Parameter	Symbol	Minimum	Maximum	Unit
IRQ delay from rising clock	t_1	-	45	nS
IRQ false from rising clock	t_2	-	45	nS

Switch Select



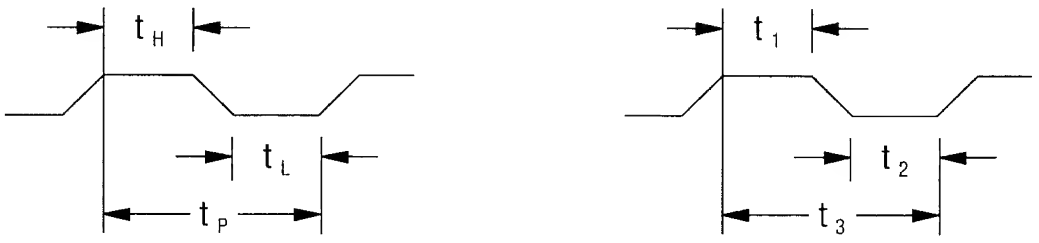
Parameter	Symbol	Minimum	Maximum	Unit
Switch select delay from RESET true	t_1	-	50	nS
Switch select false from RESET false	t_2	-	50	nS

Miscellaneous External Select Signals



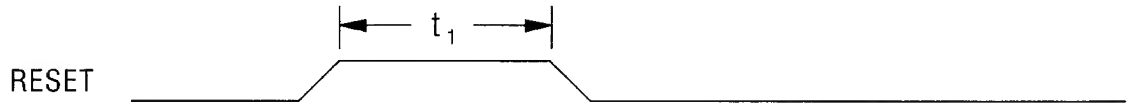
Parameter	Symbol	Minimum	Maximum	Unit
Select signal delay from SMEMR/ or SMEMW/	t_1	-	60	nS
Select false from SMEMR/ or SMEMW/ false	t_2	-	60	nS

Clock and Oscillator Timings



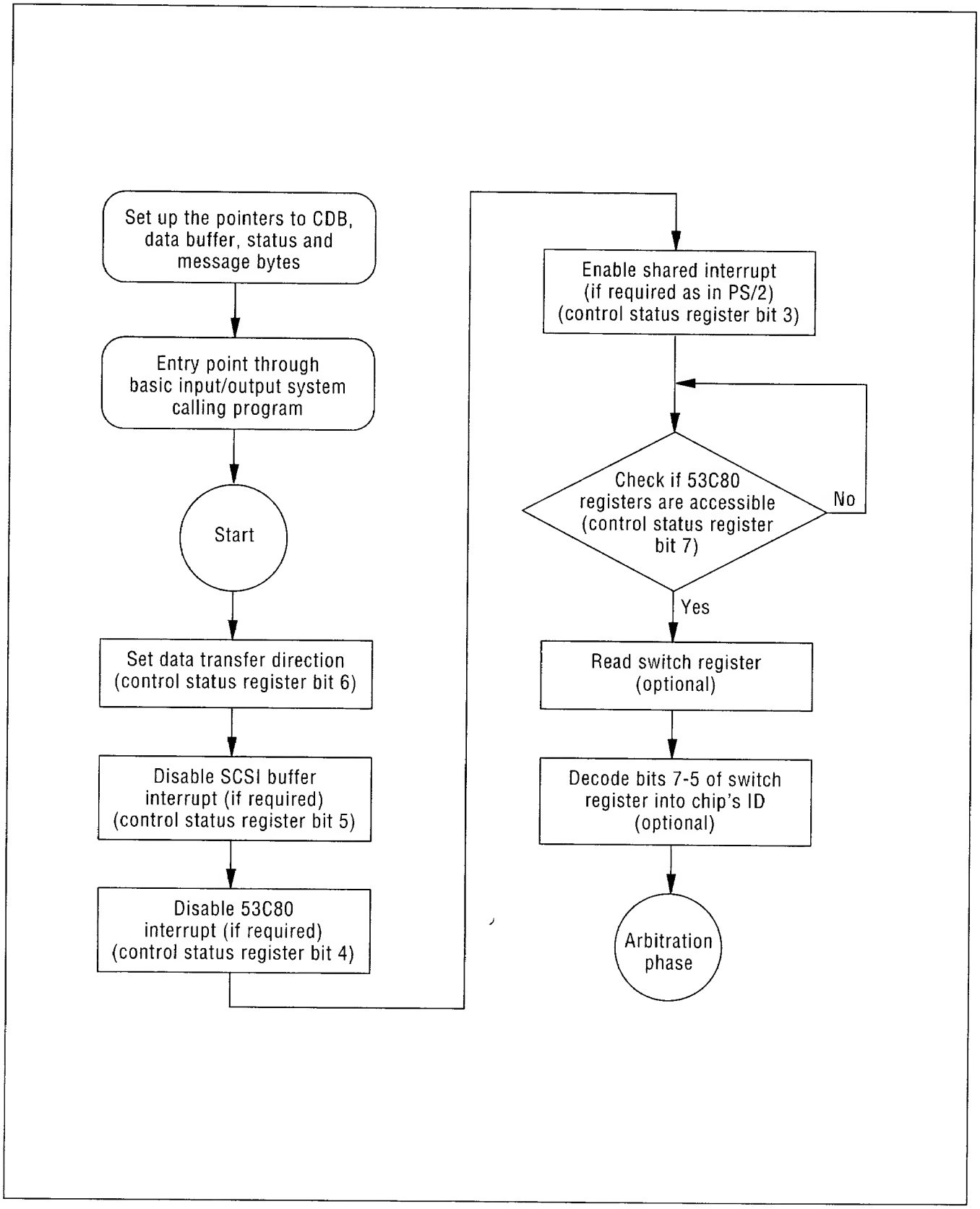
Parameter	Symbol	Minimum	Maximum	Unit
CLK high	t_H	20	-	nS
CLK low	t_L	20	-	nS
CLK period	t_P	70	210	nS
OSC high	t_1	20	-	nS
OSC low	t_2	20	-	nS
OSC period	t_3	68	72	nS

RESET Timing

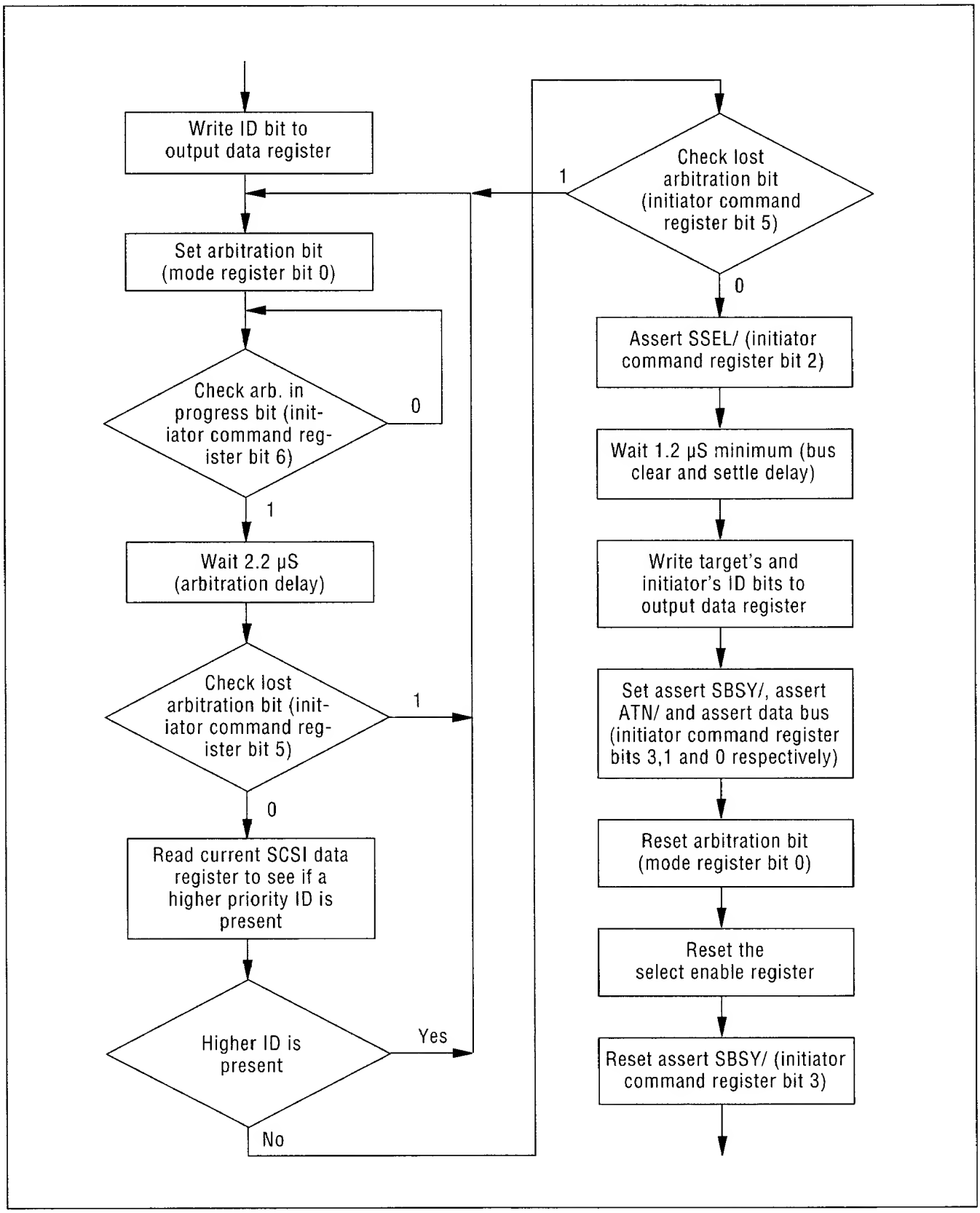


Parameter	Symbol	Minimum	Maximum	Unit
Reset pulse width	t_1	200	-	nS

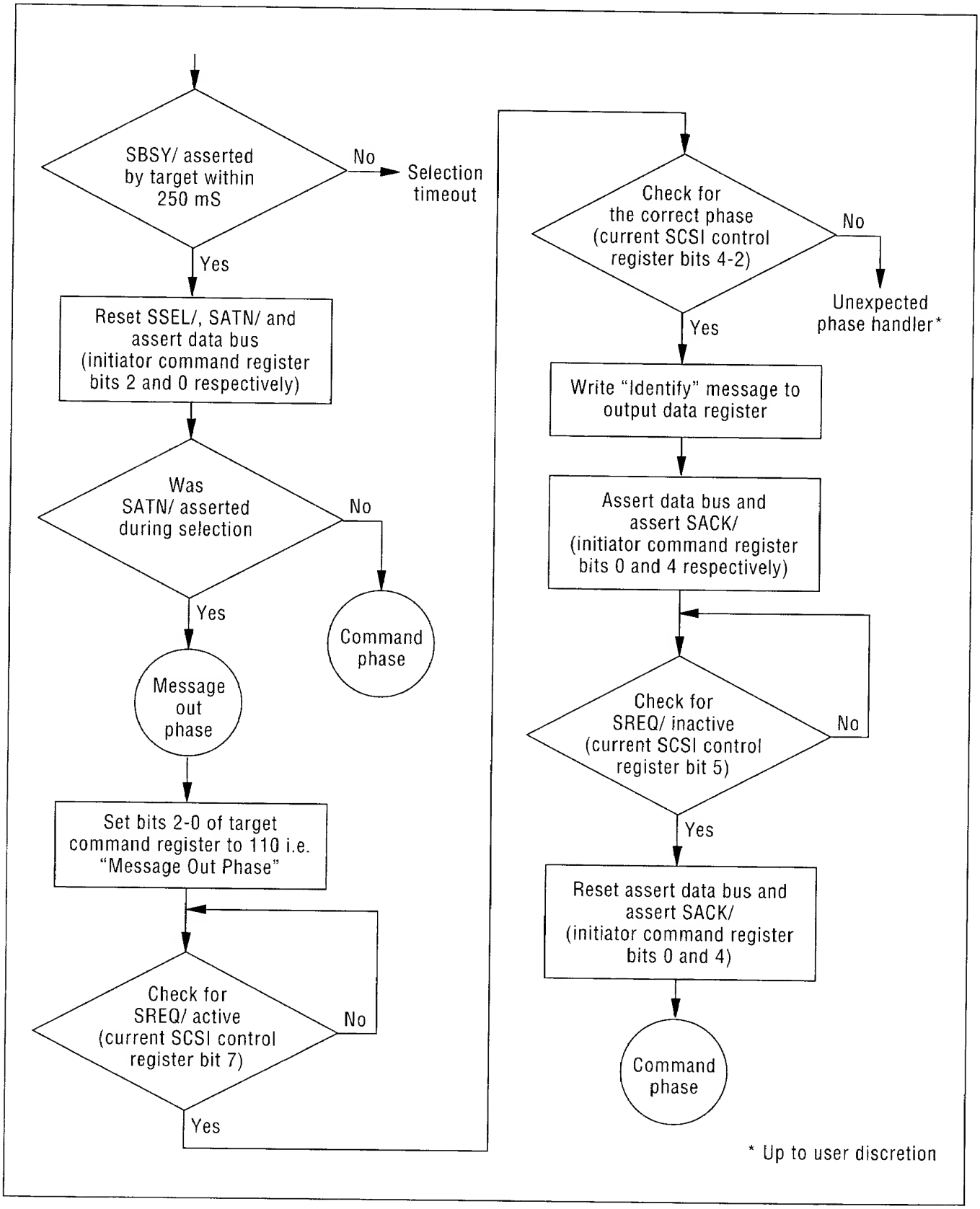
Programming Flow Chart



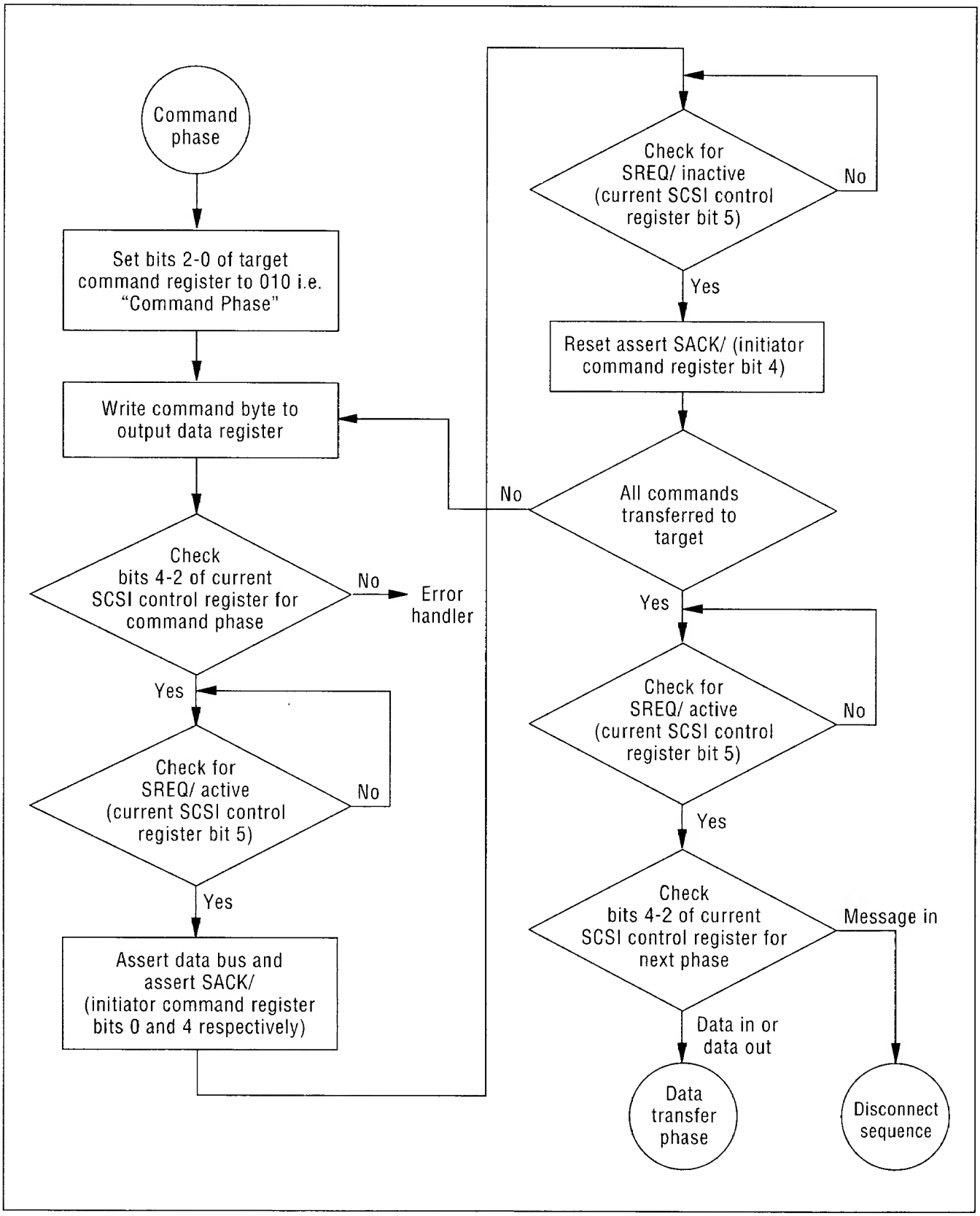
Programming Flow Chart (Con't)



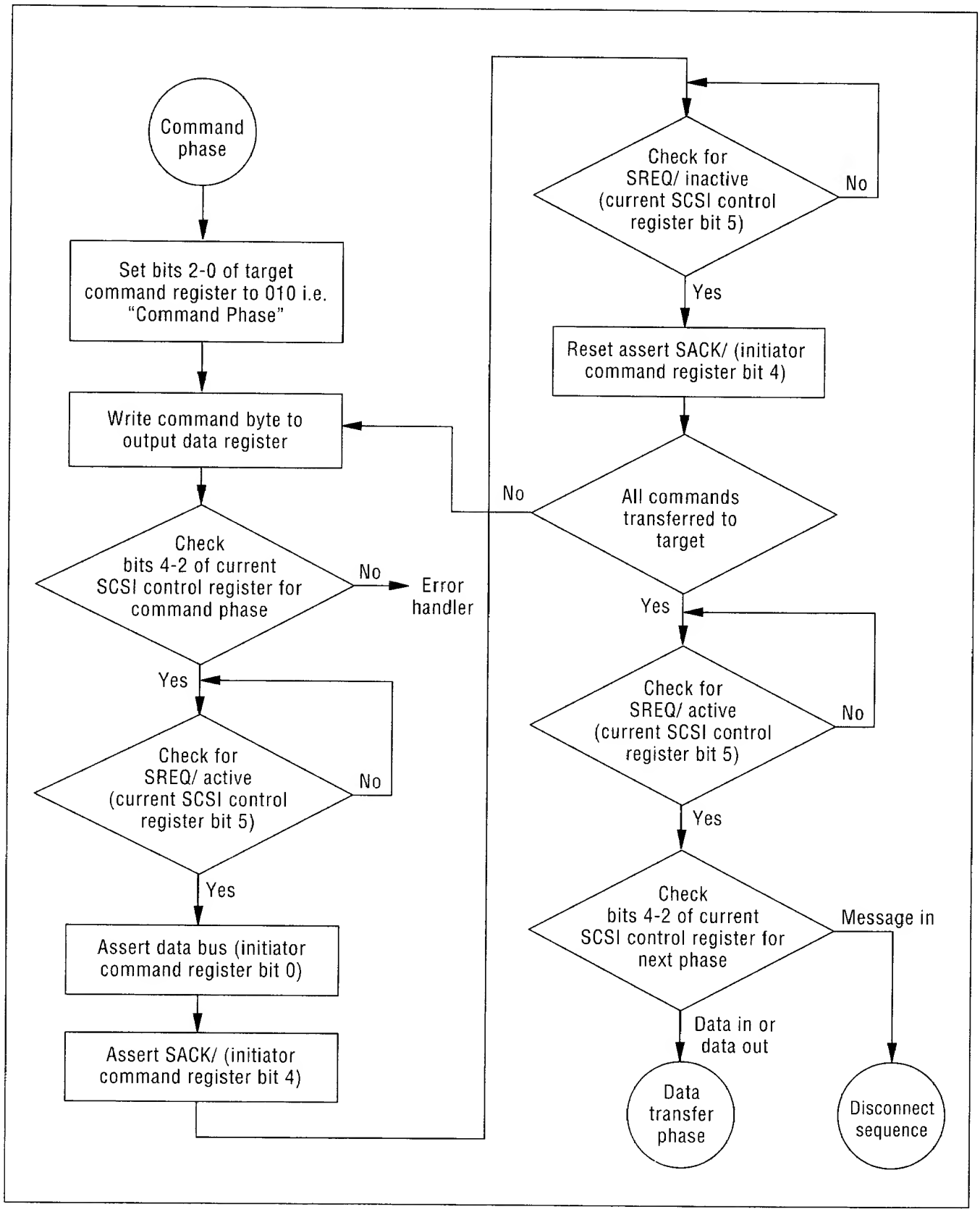
Programming Flow Chart (Con't)



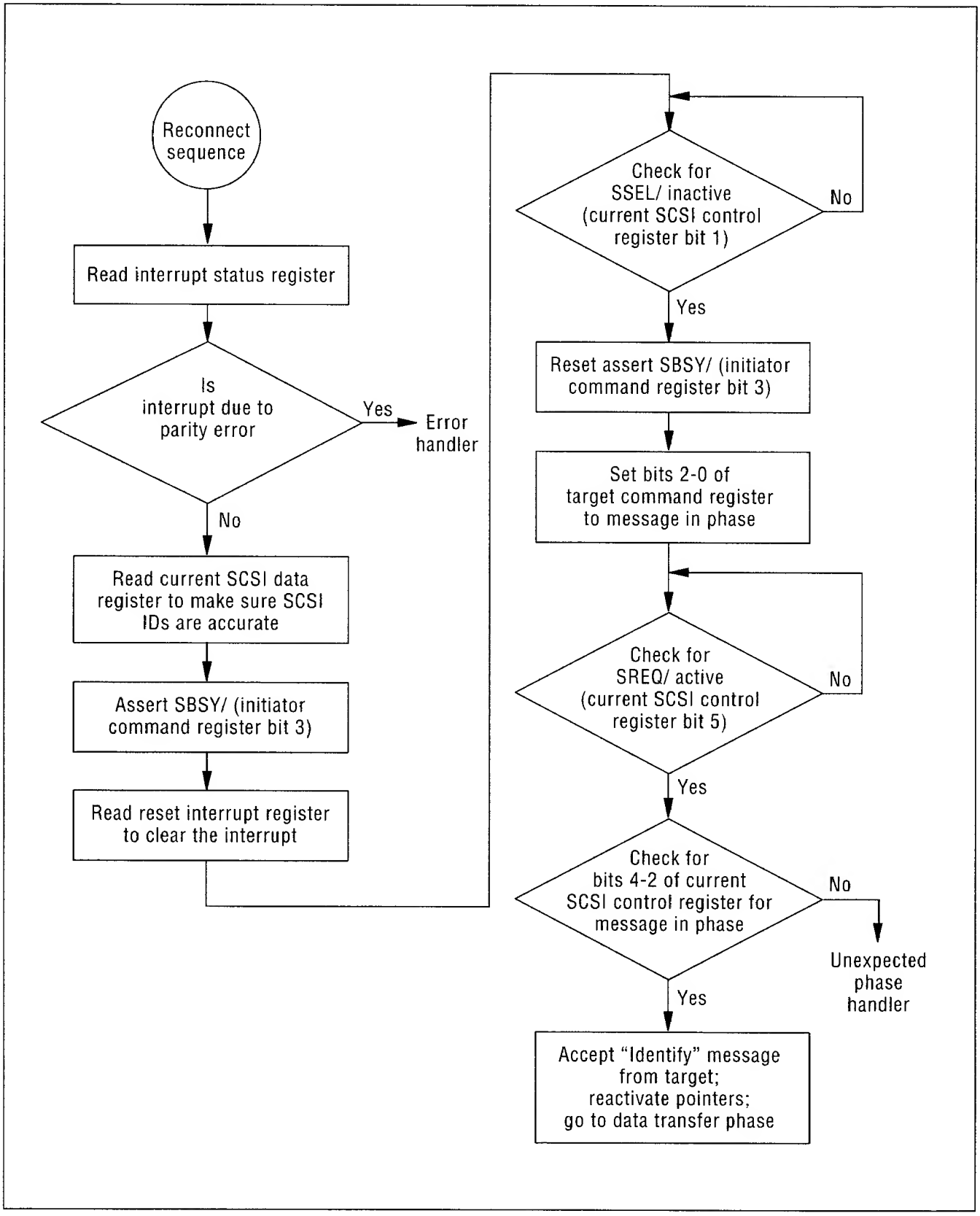
Programming Flow Chart (Con't)



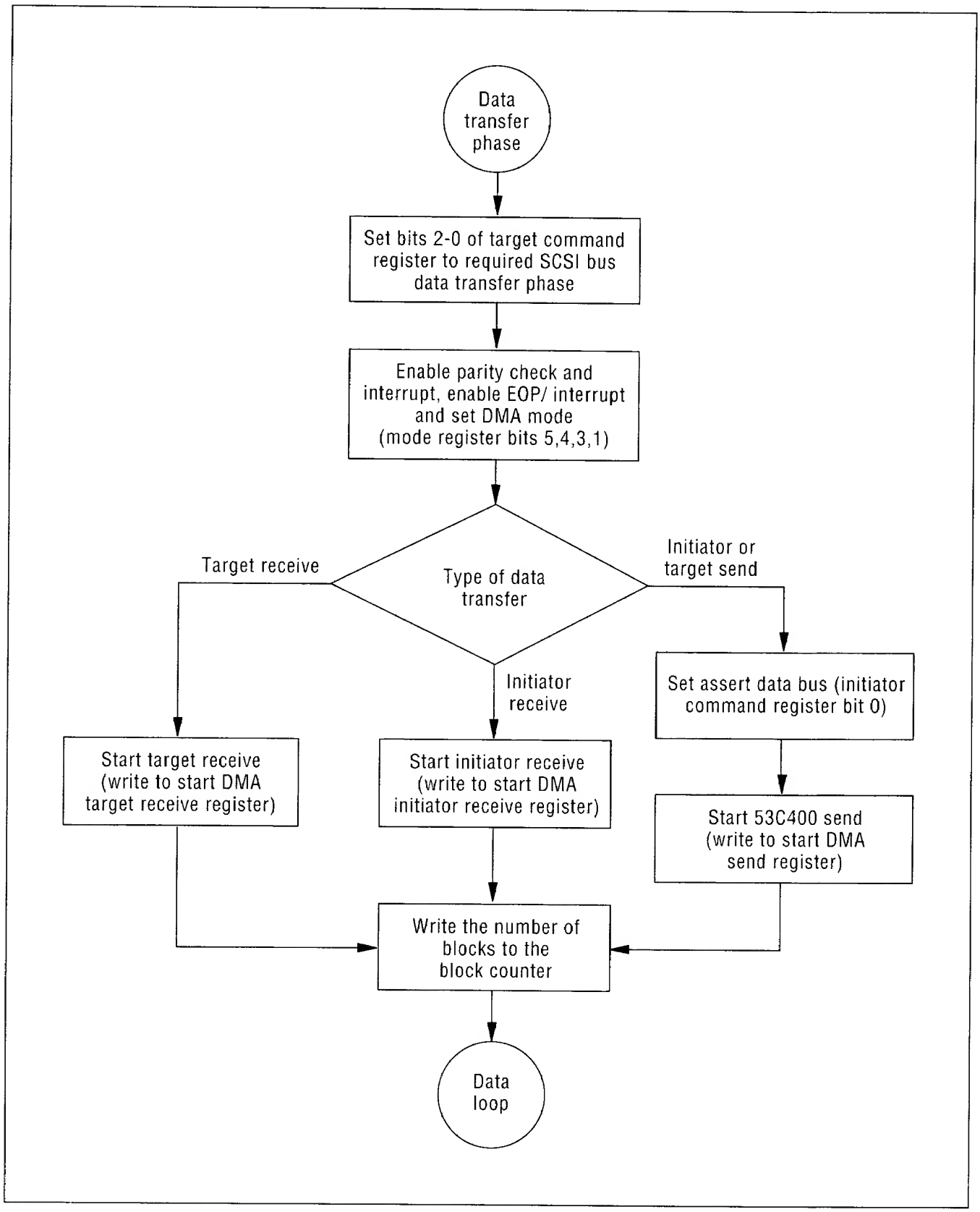
Programming Flow Chart (Con't)



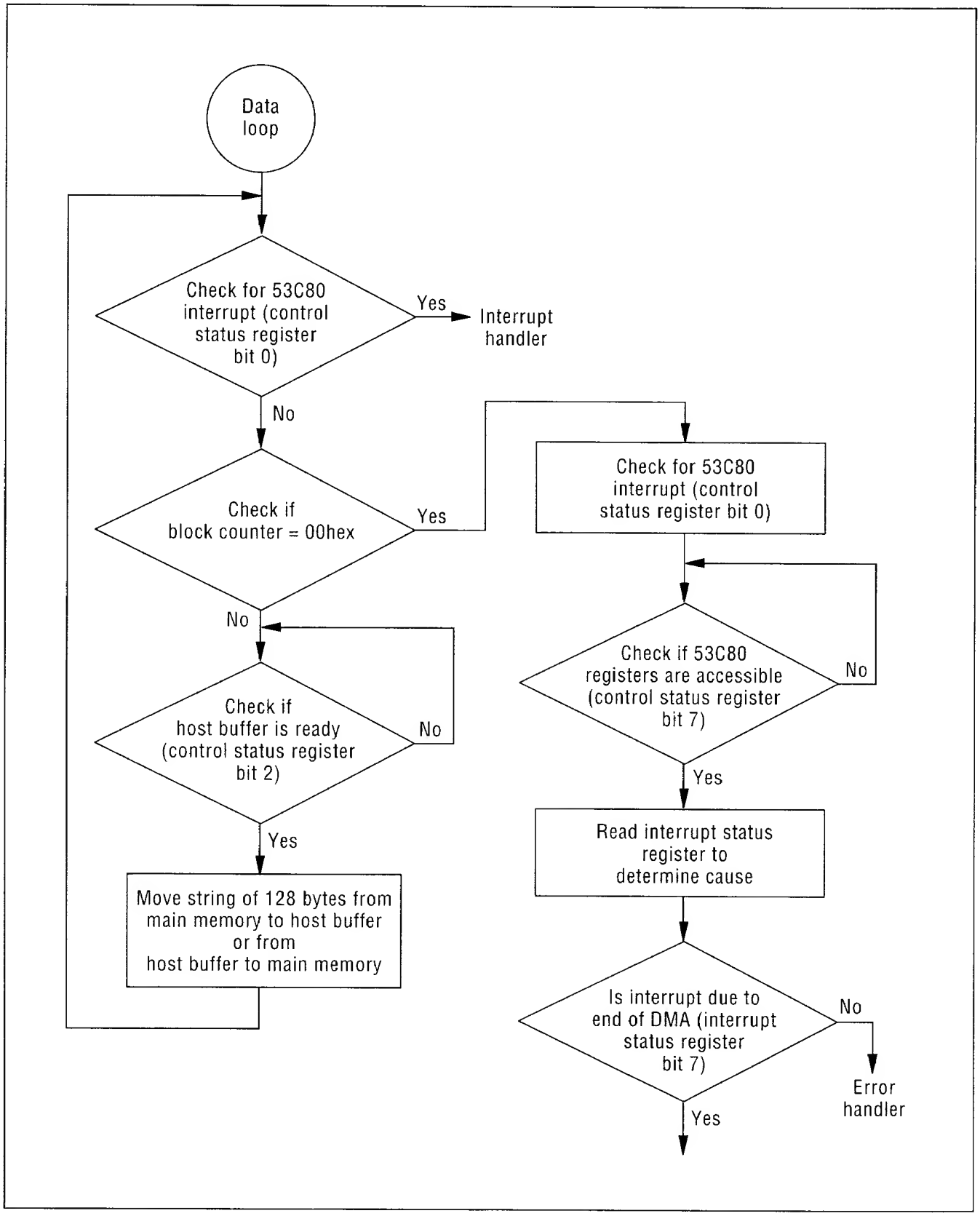
Programming Flow Chart (Con't)



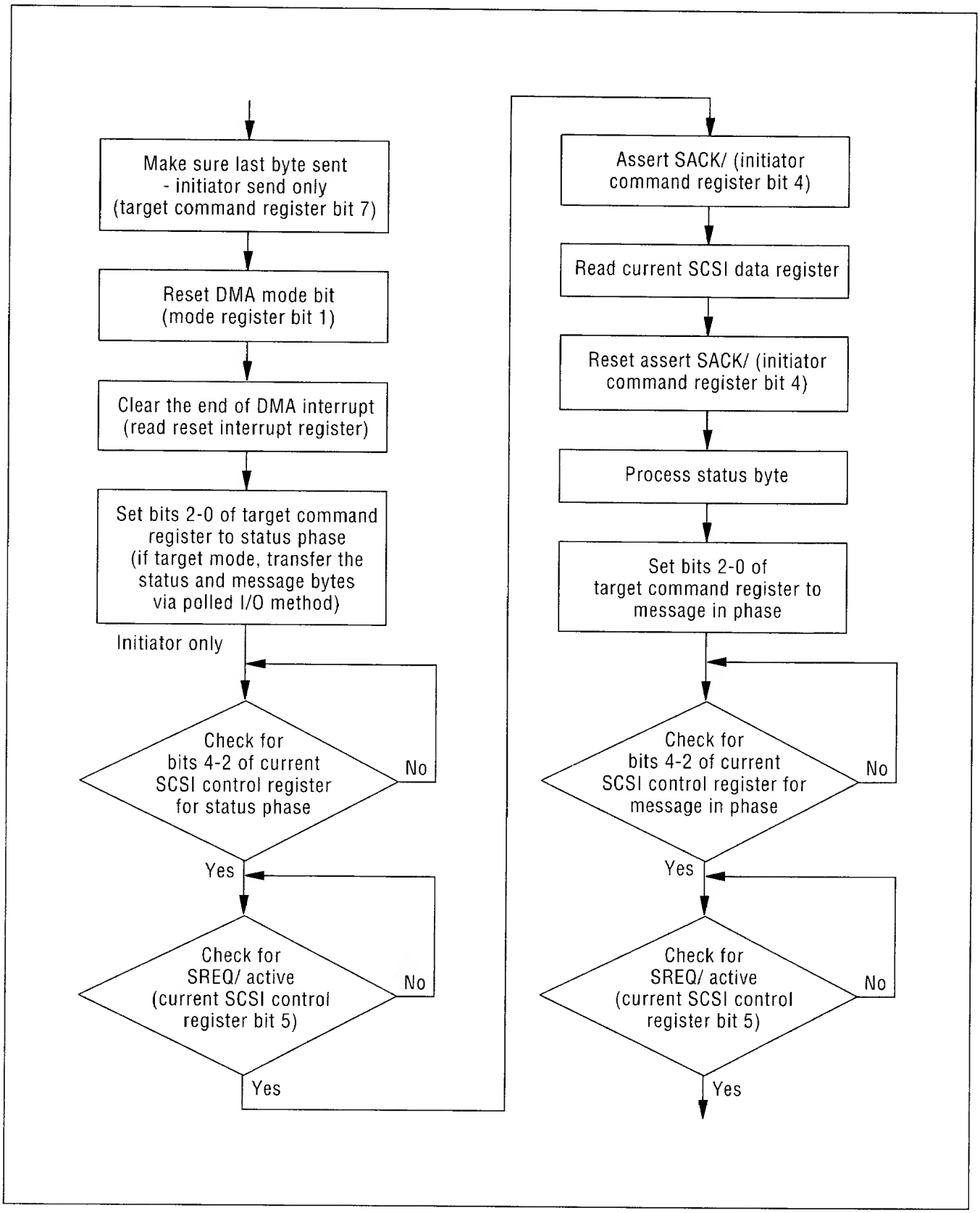
Programming Flow Chart (Con't)



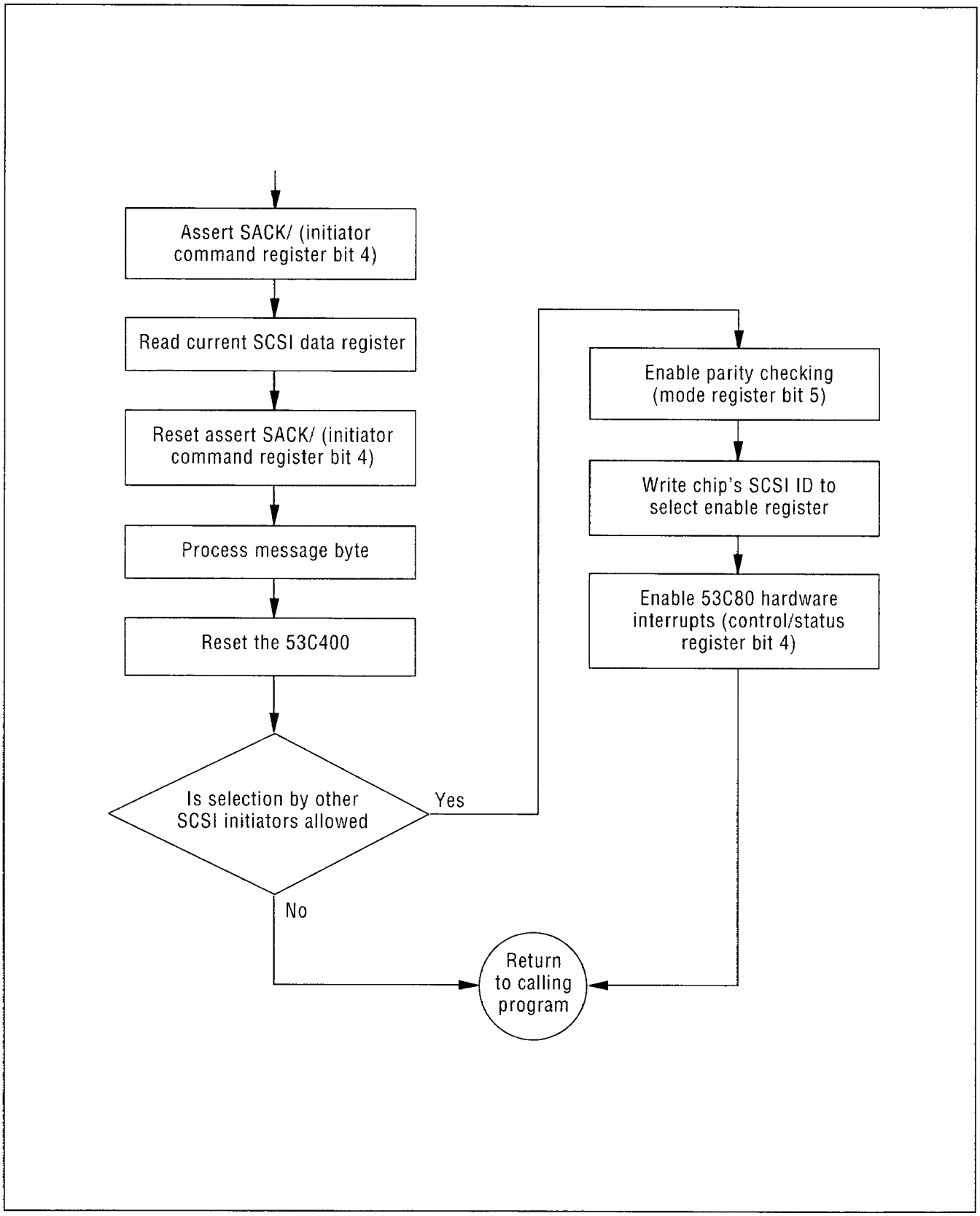
Programming Flow Chart (Con't)



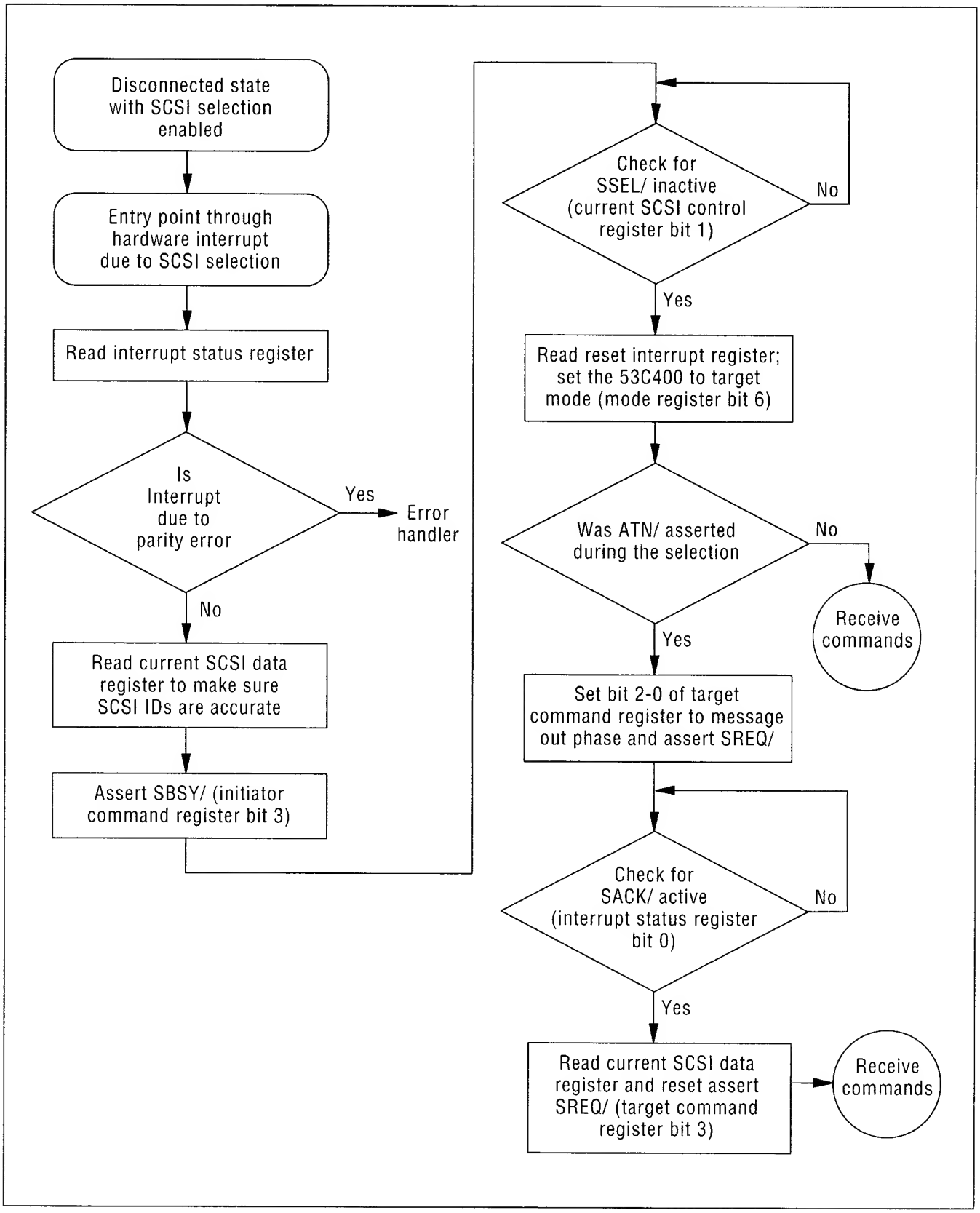
Programming Flow Chart (Con't)



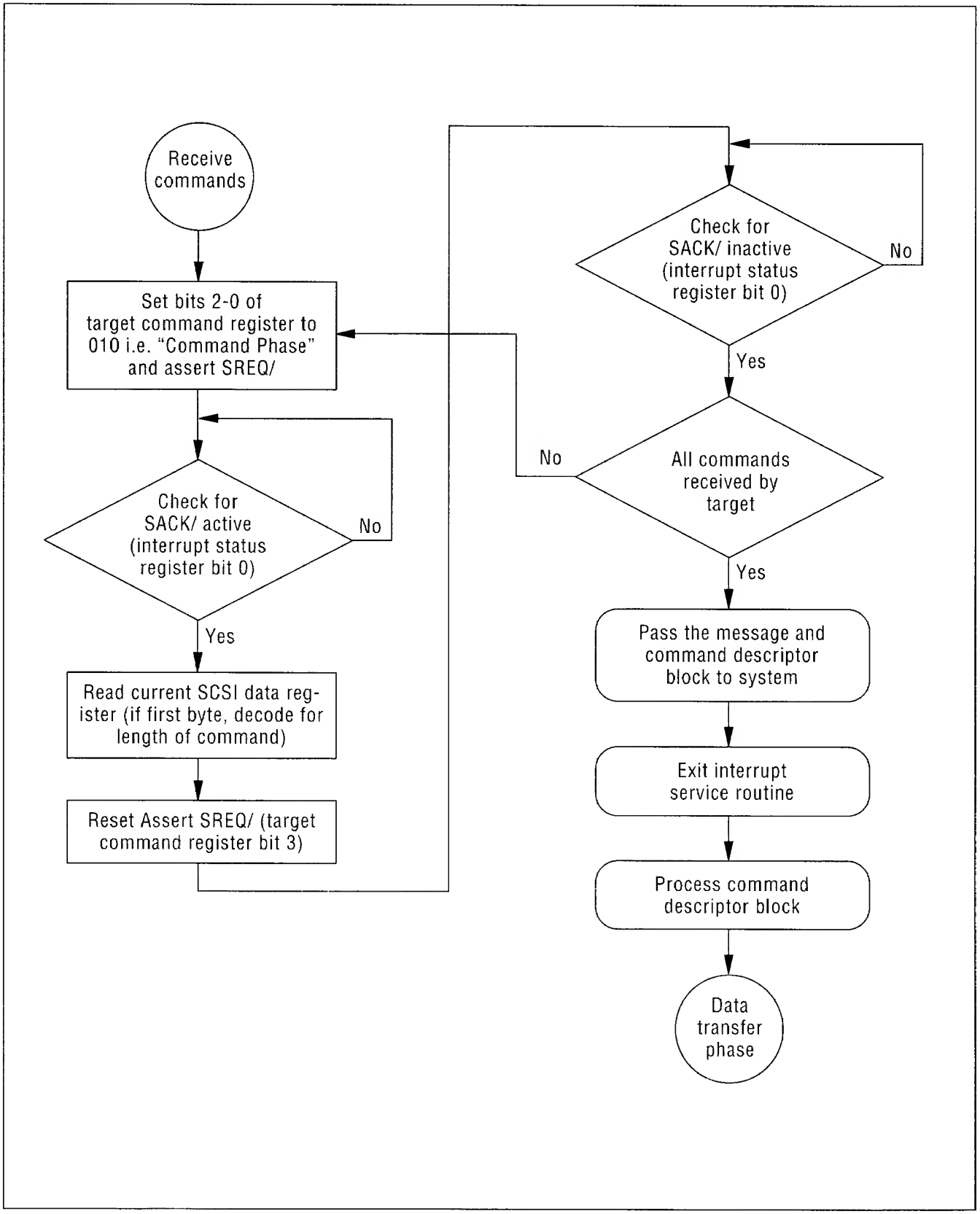
Programming Flow Chart (Con't)



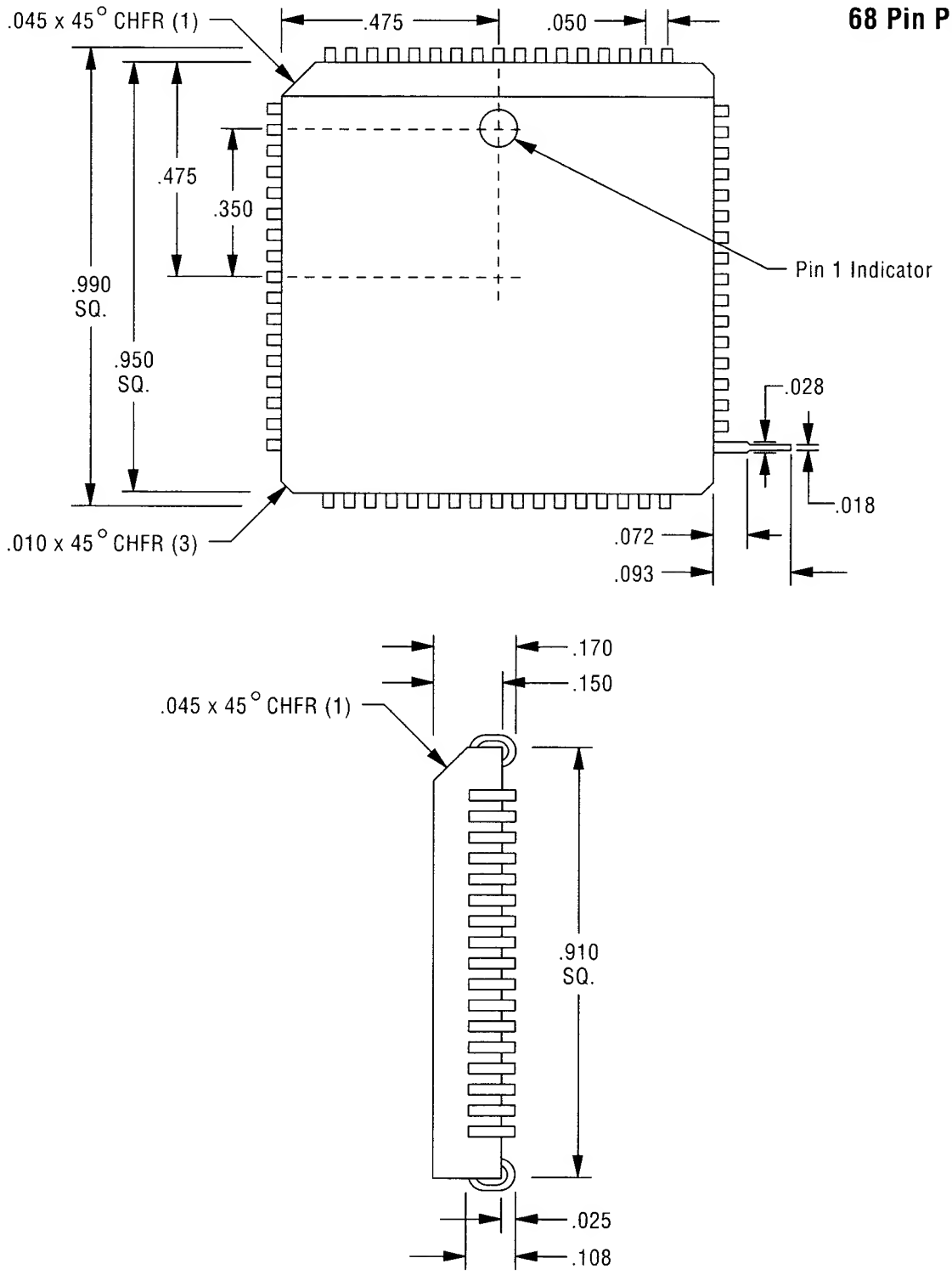
Programming Flow Chart (Con't)



Programming Flow Chart (Con't)



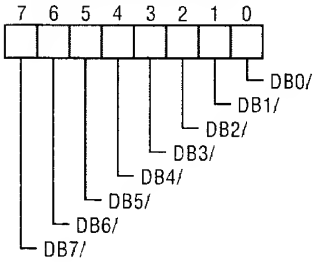
Mechanical Data



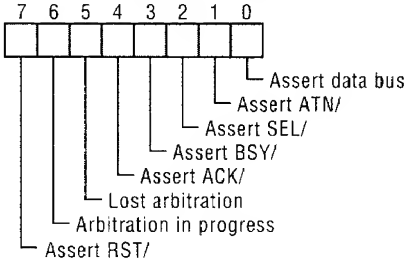
Appendix A – Register Summary

Read

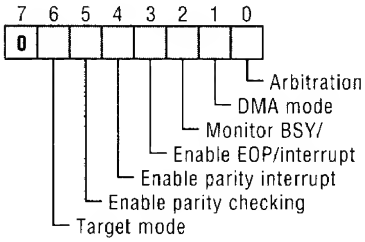
Current SCSI Data (3880H)



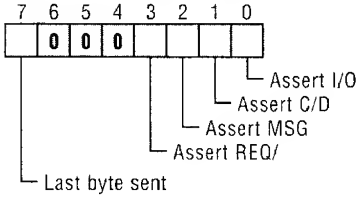
Initiator Command Register (3881H)



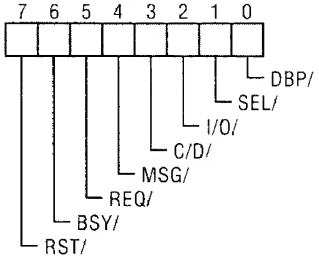
Mode Register (3882H)



Target Command Register (3883H)

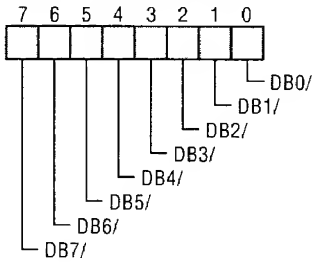


Current SCSI Control Bits (3884H)

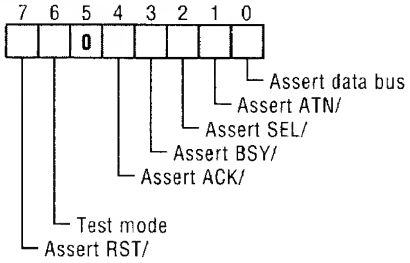


Write

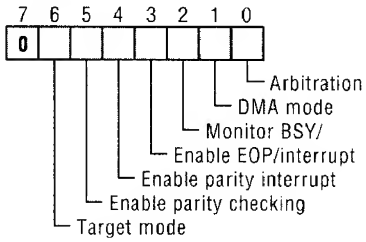
Output Data Register (3880H)



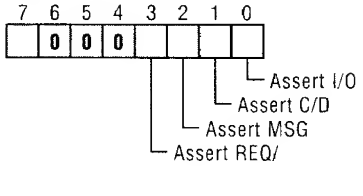
Initiator Command Register (3881H)



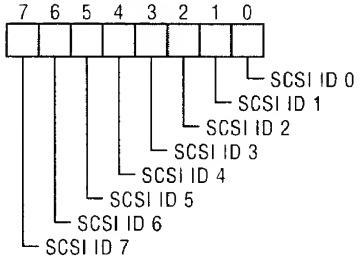
Mode Register (3882H)



Target Command Register (3883H)



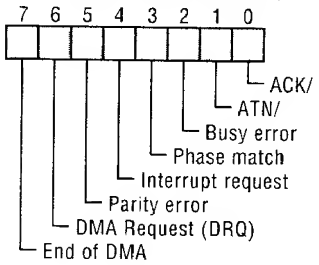
Select Enable Register (3884H)



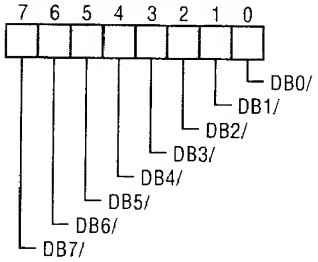
Appendix A – Register Summary (Con't)

Read

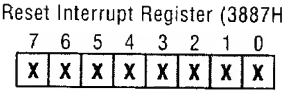
Interrupt Status Register (3885H)



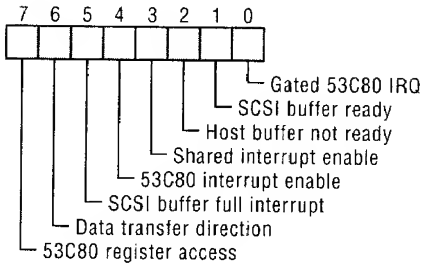
Input Data Register (3886H)



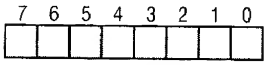
Reset Interrupt Register (3887H)



Control Status Register (3980H)



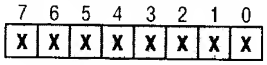
Block Counter (3981H)



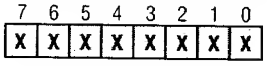
(read or write)

Write

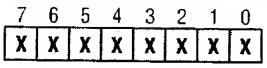
Start DMA Send (3885H)



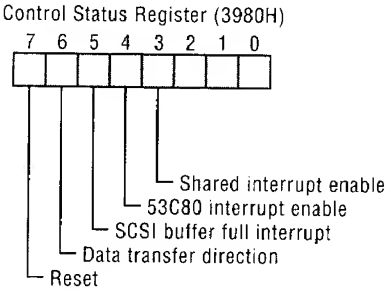
Start DMA Target Receive (3886H)



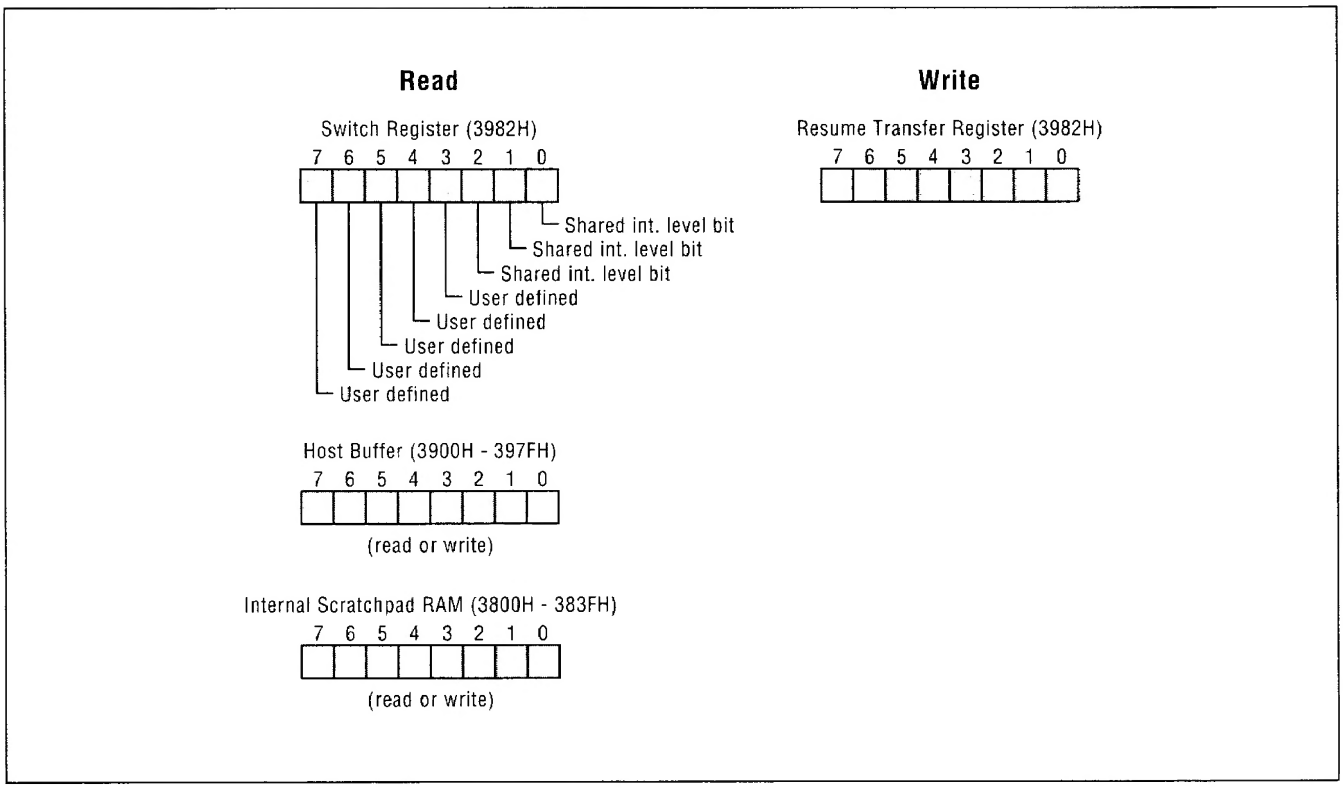
Start DMA Initiator Receive (3887H)



Control Status Register (3980H)



Appendix A – Register Summary (Con't)

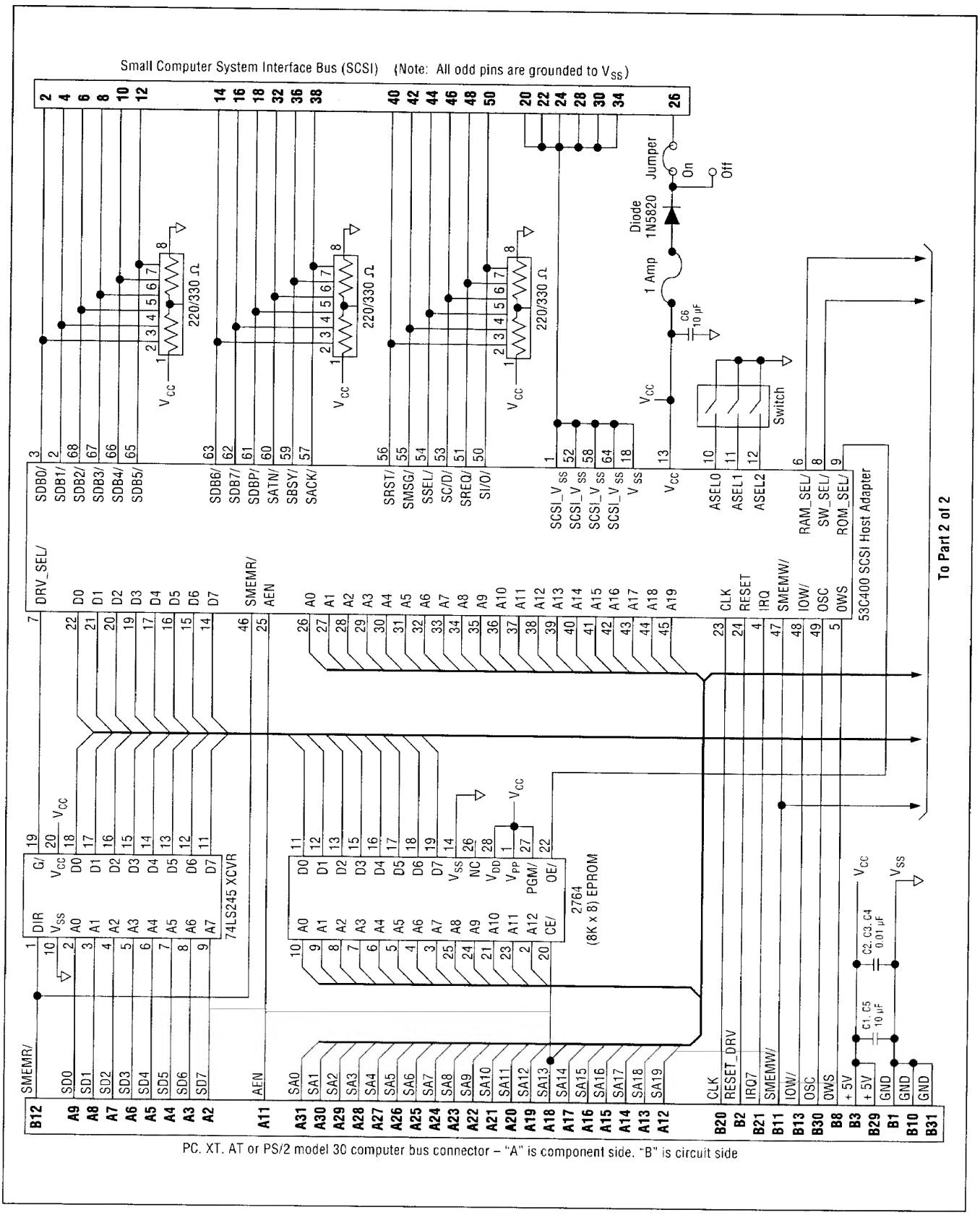


SCSI Information Transfer Phases

Bus Phase	SMSG/	SC/D/	SI/O/
Data out	0	0	0
Data in	0	0	1
Command	0	1	0
Status	0	1	1
Unspecified	1	0	0
Unspecified	1	0	1
Message out	1	1	0
Message in	1	1	1

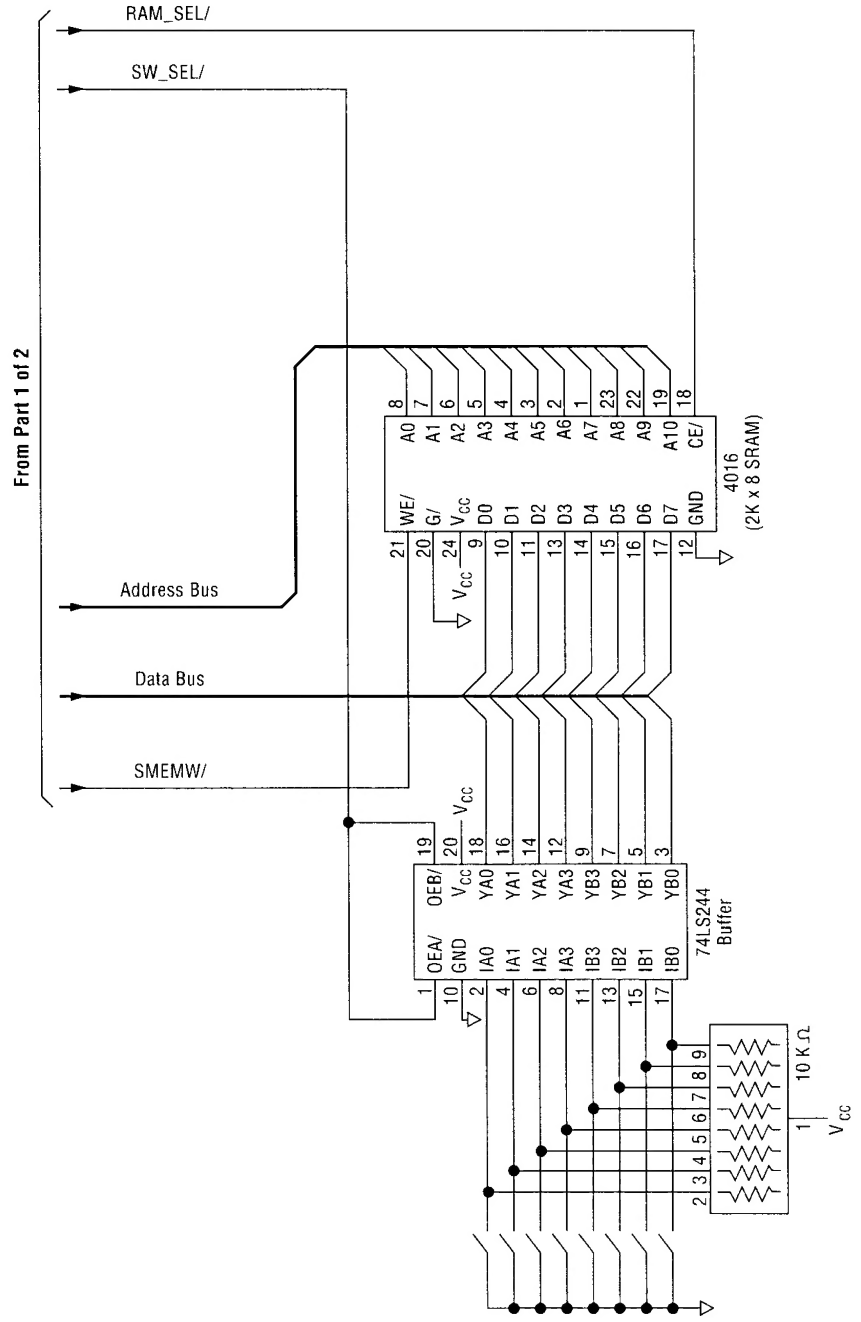
Note: *A (0) represents an inactive state and a (1) represents an active state.*

Appendix B – Host Adapter Card Layout (Part 1 of 2)



PC, XT, AT or PS/2 model 30 computer bus connector – "A" is component side, "B" is circuit side

Appendix B – Host Adapter Card Layout (Part 2 of 2)



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